ON CHIP ERROR COMPENSATION, LIGHT ADAPTATION, AND IMAGE ENHANCEMENT WITH A CMOS TRANSFORM IMAGE SENSOR

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ON CHIP ERROR COMPENSATION, LIGHT ADAPTATION, AND IMAGE ENHANCEMENT WITH A CMOS TRANSFORM IMAGE SENSOR

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SUMMARY

CMOS imagers are replacing CCD imagers in many applications and will continue to make new applications possible. CMOS imaging offers lower cost implementations on standard CMOS processes which allow for mixed signal processing on-chip. A system-on-a-chip approach offers the ability to perform complex algorithms faster, in less space, and with lower power and noise. Our transform imager is an implementation of a mixed focal plane and peripheral computation imager which allows high fill factor with high computational rates at low power. However, in order to use the technology effectively a need to verify and further understand the behavior and of the pixel elements in this transform imager was needed. This thesis presents a study of the pixel elements and mismatches and errors in the pixel array of this imager. From there, a discussion about removing offsets and an implementation of a circuit to remove the largest offsets is shown. To further enhance performance, initial work to develop light adaptive readout circuits is presented. Finally, an overview is given of a newly designed one-megapixel transform imager with many design improvements.

CHAPTER 1

INTRODUCTION

Modern CMOS imagers are opening up a new field of possibilities for image sensing and processing. CCD imagers have dominated the imaging market and produced high quality results, but they have the limitation of needing a special processes that do not allow for high levels of on chip integration. CCD's also consume require high voltage generation and require higher power then CMOS imagers. CMOS imaging technology, however, can be implemented on standard CMOS precesses. This allows standard analog and digital circuitry to be integrated with the imager sensor all on one chip. This opens many opportunities for mixed signal image processing. A system-on-a-chip approach offers the ability to perform complex algorithms smaller and faster, with lower power and noise. These designs can be prototyped and implemented on widely used and lower costing standard CMOS technology. Advancements in CMOS imaging will allow for new paradigms of imager applications. These low cost smart imagers will allow for not just image acquisition, but a complete vision systems that can be integrated in low power applications, including mobile applications.

When designing a computational imaging system, several approaches may be taken. There are many choices when dividing work between digital and analog domains. Several architectural options are available which can be tailored to the particular computational task at hand. Making the array of choices even larger is the notion of focal plane processing. Focal plane processing is a biologically inspired approach which moves some computational circuitry from the periphery of the sensor array to the pixels themselves. Our implementation of mixed focal plane and peripheral computation allows high fill factor with high computational rates at low power. In order to use the technology effectively a need to verify and further understand the behavior and of the pixel elements was needed. In particular, certain offsets and mismatches which are inherent in CMOS technology effect our results

and need to be compensated where possible. The goal of these studies is to help direct designs for better imagers. An additional goal of this research was to gain an understanding CMOS imaging and to understand what most immediate issues are at hand for implementing a successful vision system. Previous work has been done to verify the concept of the architecture used, but in order to improve results investigations into the operation of the system was needed to guide efforts for improvement. First, in Chapter 2, an introduction to CMOS imagers is given, including an introduction to the transform imager used in this research. Then, Chapter 3 presents a study of the pixel element operation and mismatches among pixels in an array. Chapter 4 shows an approaches to removing offsets and Chapter 5 presents some work done toward implementation of light adaptation to enhance imager performance. Chapter 6 presents the design a larger one-megapixel imager and finally a conclusion is presented.

CHAPTER 2

CMOS IMAGERS

CMOS image sensors offer a lot of flexibility in design . As with most sensors, there are several circuits which must be designed to properly extract the information from the image sensor. Then there are typically digital control circuits, which can all be integrated on chip to produce a camera-on-a-chip [1]. From there, signal processing circuits can be integrated on chip. A variety of choices are available for each part as well as the system architecture. This chapter will introduce some photoreceptor circuits and imager technologies including active pixel sensors (APS), which dominate the CMOS imaging market, and the transform imager architecture that is used for the body of this research[2, 3].

2.1 Basic Photoreceptor Circuits

The basic photoreceptor is the reverse biased PN junction. When photons strike near the junction they create electron hole pairs. The energy carriers created can cross the junction, assuming that recombination does not occur first. A small electric field in the junction helps the electrons cross the barrier. This photon induced current flow is what is used for measuring the light intensity at the sensor. In this structure the current flow is proportional to the number of photons that fall on the junction. This allows the photodiode to act in a circuit as a light controlled current source. It is not a perfect current source since the voltage across the junction effects the current flow as well, though its effect is relatively small. A similar effect is also seen using a NFET as a current source, which has current flow controlled by not only the gate to source voltage but also the drain to source voltage. This is called the early effect in transistors and is modeled in as a resistor in parallel to the current source in a small signal model. A similar resistance is used in a model for a photodiode [4] and a diode.

To use the current from the photodiode, a current amplification or I-V conversion usually must be performed. Figure 1 shows some basic photoreceptor circuits. Figure 1 (a) shows the basic current flow , I_{photo}, which is proportional to the light falling on the reverse biased PN junction. Figure 1 (b) shows a photodiode used as a current source in a source follower configuration. To understand the behavior of this configuration, one must realize that the current flowing through the photodiode in typical imaging applications is in the order of nanoamps and picoamps. This current flow though an NFET mandates a sub-threshold analysis of the circuit. In sub-threshold we have a current flow through the transistor described by Equation 1.

$$I_D = \frac{W}{L} I_t e^{-\frac{V_t}{U_t}} e^{\frac{\kappa V_g - V_s}{U_t} - \frac{\kappa V_g - V_d}{U_t}} \tag{1}$$

Since the source voltage appears in an exponential term in the current equation, the output of this circuit will change logarithmically with changes in current. Outputs that are logarithmically related to inputs have an effect which is often desirable: logarithmic compression. This means that the circuit can handle inputs changes over several orders of magnitude while keeping the output changes at reasonable levels. Imaging applications often face light levels that vary in several orders of magnitude, even in the same image. Logarithmic compression can allow successful capturing and processing of these widely varying light intensities. Figure 1 (c) shows a more typical logarithmic photoreceptor which uses a diode connected PFET to give a voltage output that is logarithmically proportional to the light level. The last circuit, illustrated in 1 (d), shows the most widely established CMOS imaging technology, the Active Pixel Sensor or APS. This circuit takes advantage of the capacitance of the PN junction. The reset transistor resets the capacitor leaving it in a charged state. The reset transistor is then turned off and the photodiode drains the capacitor at a rate proportional to the light level. The voltage on the capacitor is actively buffered through a source follower configuration.

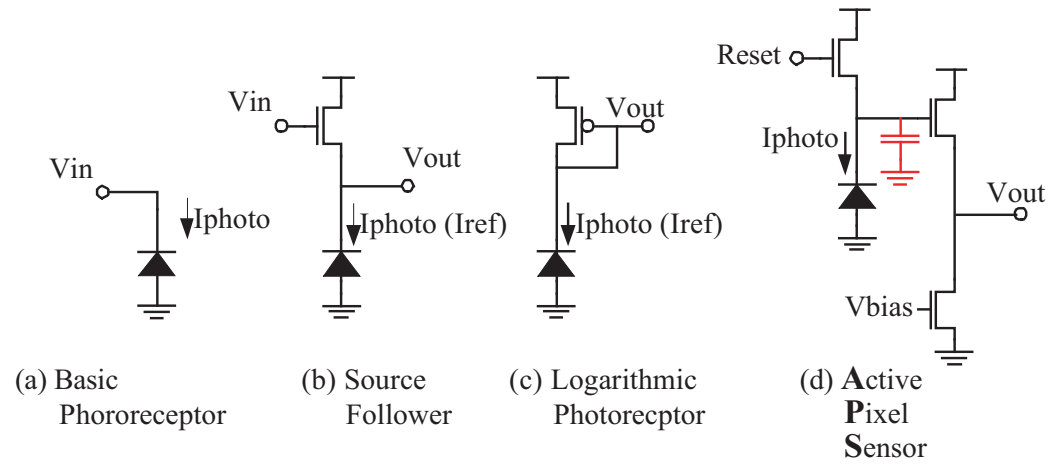


Figure 1. Some basic photoreceptor circuits.The basic photoreceptor (a) is a reverse bias PN junction which conducts a current proportional to the amount of light falling on the junction. The photoreceptor can be used as current source in configurations like the source follower (b) and the logarithmic photoreceptor (c) which both perform logarithmic compression in the current to voltage conversion. The Active Pixel Sensor (d) configuration uses an active amplifier to generate the output. In the APS circuit the current is integrated on an implicit capacitor and that voltage is given to the active amplifier.

2.2 Active Pixel Sensors (APS)

APS is a good place to start when examining CMOS imaging technology since it is widely used. To evaluate the technology, a APS pixel was fabricated and tested. The layouts is shown in Figure 3. This layout includes the row select transistor needed for use in an array. Typically, the NFET bias transistor for the output amplifier is shared for a column of pixels as illustrated in Figure 2.

Light filters where used to test the response of the pixel. Figure4(a) shows the transient voltage of the APS. The initial jump in voltage occurs with the reset signal. When the reset signal is lowered, a capacitive coupling and charge feed-through lower the voltage on the diode capacitor and is observed as a sudden small drop on the output voltage. Following this drop is the expected integration of the current of the photodiode on the capacitor causing the voltage to fall. Using light absorption filters, the light was varied to produce seven levels of light that vary by two orders of magnitude. The brightest light occurs when using no filter and is denoted by 100% transmission. The lowest light level is created using a light filter that passes 1%. As expected, the integration slope is linearly proportional to the

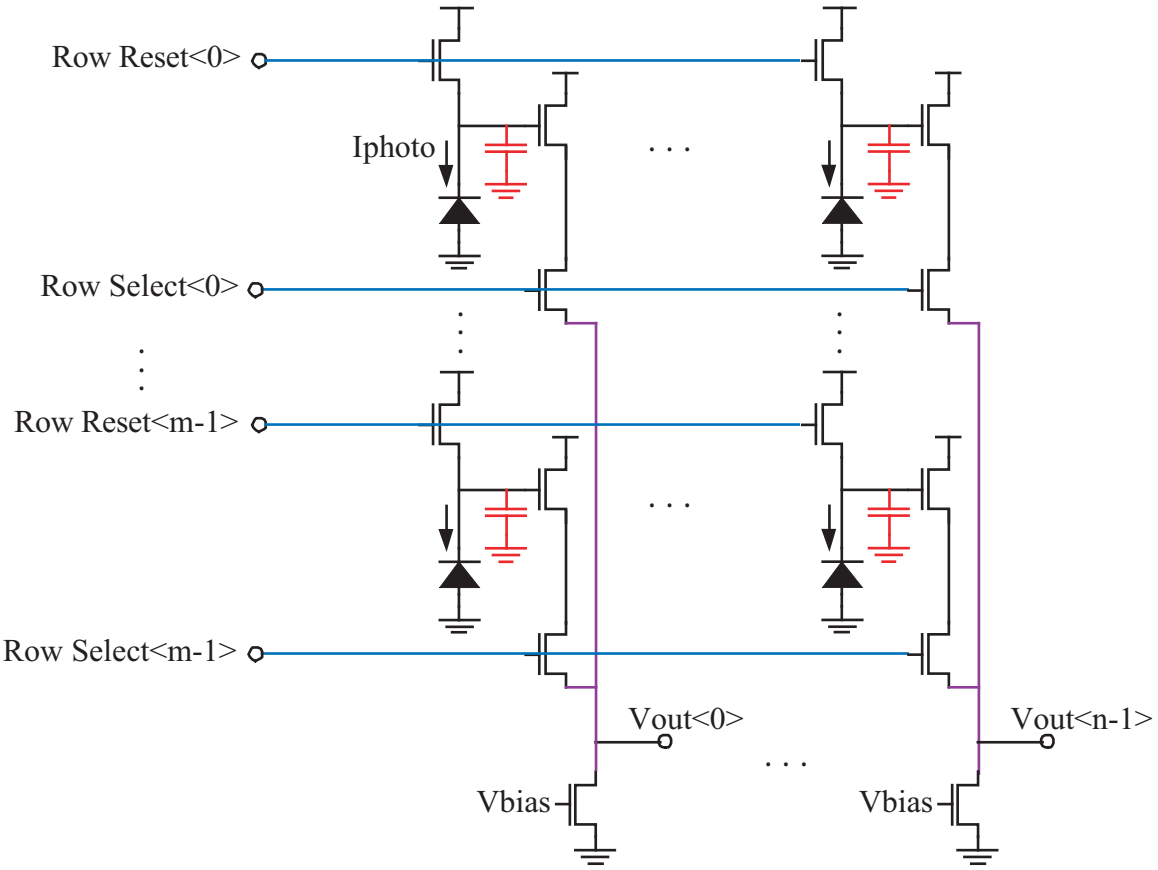


Figure 2. APS (Active Pixel Sensor) Array

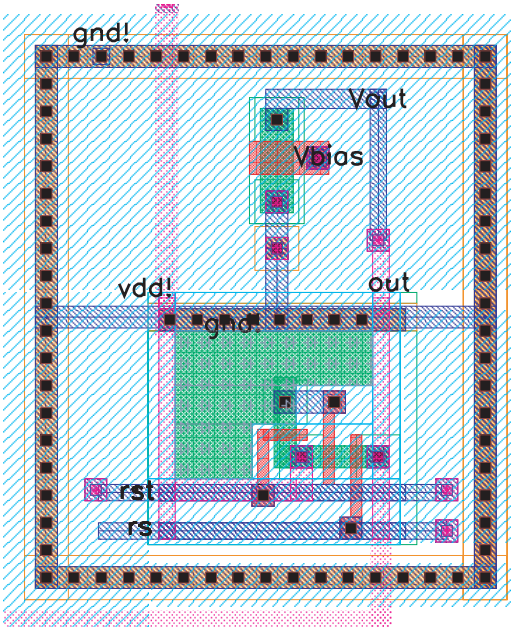


Figure 3. APS pixel layout. Here rs is a row select signal and rst is reset.

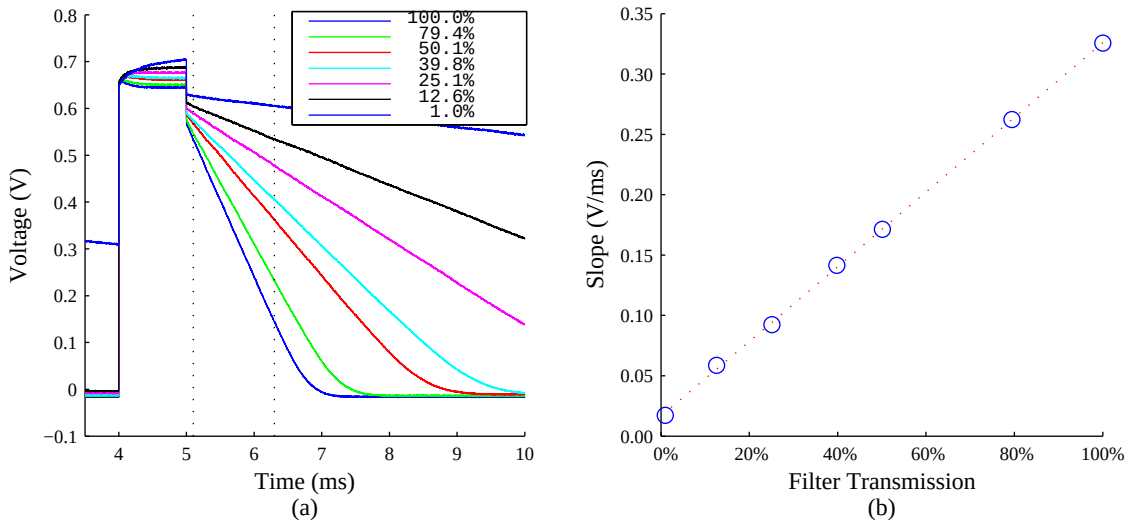


Figure 4. Measured APS pixel operation. (a) APS transient curves with varying light using light filters. (b) Extracted slopes

light intensity falling on the photosensor. The vertical dotted lines in Figure 4 (a) denote the region of the slope fit and the results are shown adjacently in 4 (b). An entire APS array was also fabricated but there seemed to be issues along columns that could not be resolved. It appeared as if pixels could not be turned off so proper operation was not achieved. The notion of pixels not turning off became important in later testing of the matrix transform imager architecture presented later.

2.3 Focal Plane Processing

Neuromorphic VLSI is field where circuits and systems are designed that in some way mimic behavior or structure of biological systems. In the neuromorphic community, focal plane processing became a focal point for a lot of research. Focal plane processing allows movement of some processing traditionally done in post DSP hardware to the level of the pixel itself. This offers some unique advantages. This approach can be illustrated by an example application: edge enhancement. High pass filtering can be achieved with a simple two-dimensional convolution, as with many other image processing techniques. At each point in an image, an kernel is applied and a resulting value is associated with that point.

To illustrate this, 3x3 kernel is assumed. A normal sampling of an image involves a very simple kernel:

$$K_{identity} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2}$$

which simply results in an output exactly matching the image data at every point. A more interesting kernel is the spacial high pass filter which results in a high pass version of the input image:

$$K_{identity} = \begin{bmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix} \tag{3}$$

A very useful kernel is obtained from the combination of the two, the edge enhancement kernel:

$$K_{edge\_enhace} = \begin{bmatrix} -1 & -1 & -1 \\ -1 & 9 & -1 \\ -1 & -1 & -1 \end{bmatrix} \tag{4}$$

The summation of the elements of the edge enhancement kernel is one, which preserves the energy from input to output. The negative coefficients mean that each data point of the output is proportional to the image element at that point and inversely proportional to the image elements around it. Conversely, it can be stated that each image element contributes positively to the local output while inhibiting the outputs of the elements surrounding it. This notion exists in biology and is called lateral inhibition, which actually occurs inside the retina. The result is an image with enhanced edges as seen in Figure 5. A sample focal plane processing approach to an edge enhancement is shown in [5]. Since edge enhancement involves local interactions of image elements, placing circuitry at the pixels

themselves has certain architectural advantages. In Figure 6, two approaches are shown for implementing the edge enhancement. In a traditional digital approach, computing the convolution at the center element requires that all nine data values must be read and stored in memory. Then the memory accessed as calculations are performed to produce the final result. One could avoid a large memory at the cost of having to read each pixel value multiple times. In the second approach the convolutions are calculated in parallel at each pixel and the result is read directly off the pixel array. Placing computational elements in the pixel comes at the cost of a reduced fill factor, which is the percentage of each pixel used by the actual photosensor. The non-photosensor area of the pixel is sometimes referred to as a "dead" region [6]. The advantage is the elimination of the digital memory and processor which typically consume more power for the same level of computation. If more processing must be done, the second scheme nicely segments the computations. This hierarchy of computation is also similar to that seen in biology. The disadvantage typically with focal plane processing is that the pixels must be made larger, reducing spacial resolution, or the photosensitive portion of the pixel must be reduced, reducing fill factor. Some neuromorphic imagers have fill factors less then 5% meaning that less then 5% of the pixel layout is photosensitive.

2.4 Matrix Transform Imager

The matrix transform imager is a design which retains a neuromorphic quality by performing computations at the pixel level, but the circuitry is kept minimal enough to retain hill fill factors of other sensors such as APS. The core pixel element is shown in Figure 7. Essentially we have a photodiode acting as current source for a differential pair. This low transistor count allows a multiplication at the pixel level in a minimal space. Remaining control and computational circuitry is placed on the periphery.

Figure 8 shows the computational flow of the architecture of the imager. The computation performed is $V*I*U$, where I is an n by n block of the image and U and V are matrices

Figure 5. Edge enhancement image

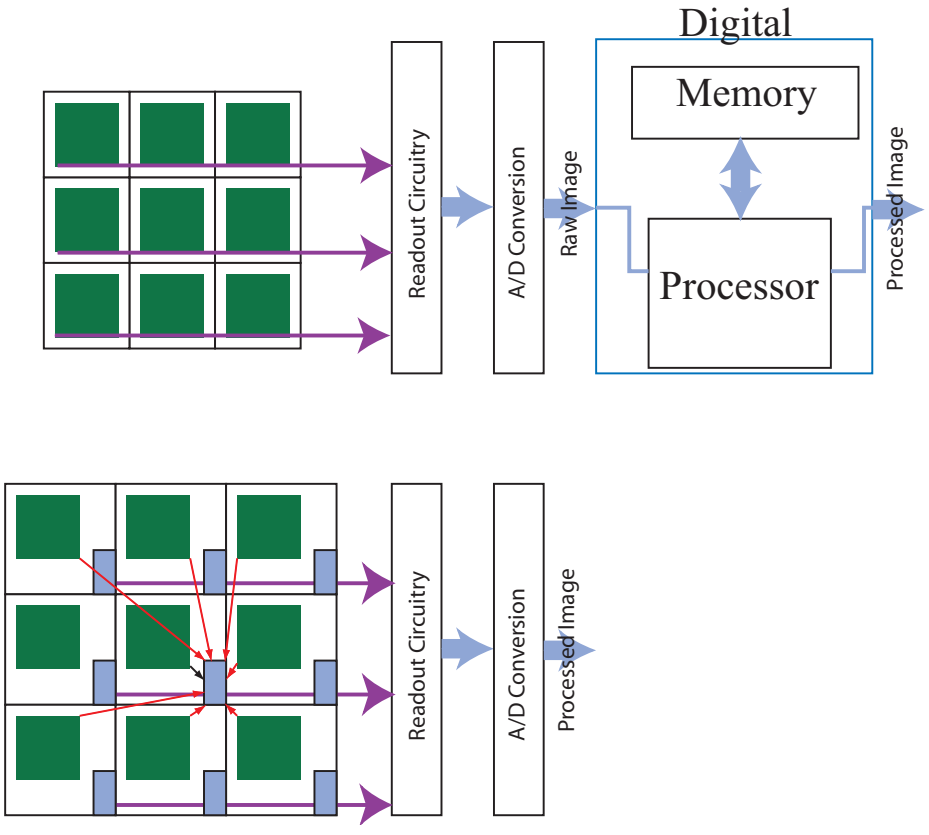


Figure 6. Architecture of traditional vs. focal plane processing

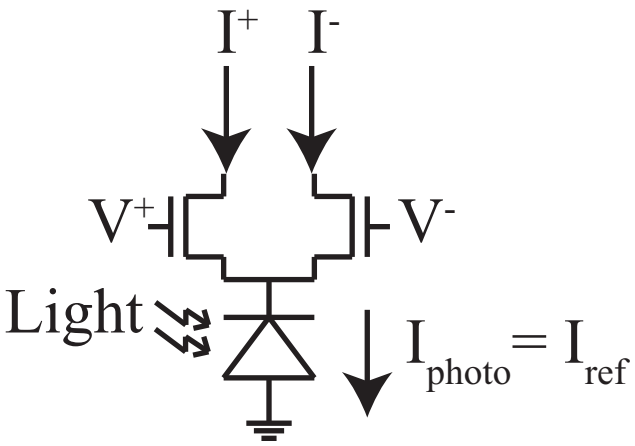


Figure 7. Differential pixel

of the same size. The elements of V are presented as a difference of two voltages as and are stored using an analog floating gate array. To compute the first column of the result, the first row of V is selected and the differential voltage vector is presented to the block of the pixel array. At each pixel in a column, a multiplication of light and the differential input is performed. Along a column, pixel outputs are tied together to get a summation of currents. This results in a dot product of the input with the column of light intensities. Each column performs this computation in parallel so that $v_1 * I$ appears at the output of the pixel block as differential currents. This vector is then presented to a vector matrix multiplier [7] that computes $v_1 * I * U$, which is the first column of the final result. To compute the other columns of the result, the remaining rows of V must be selected in turn. Figure 9 shows a complete imager with row selection. In the imager, only one row of blocks is selected at a time so the procedure must be repeated for each row of blocks in the pixel array. If the vector matrix multiplier is duplicated, multiple block results can be computed in parallel, otherwise the column block selection must scan through the imager one at a time. Though this specific design computes transforms on blocks of the image, the architecture is flexible enough to be modified to perform more general separable convolutions, as well as other computations.

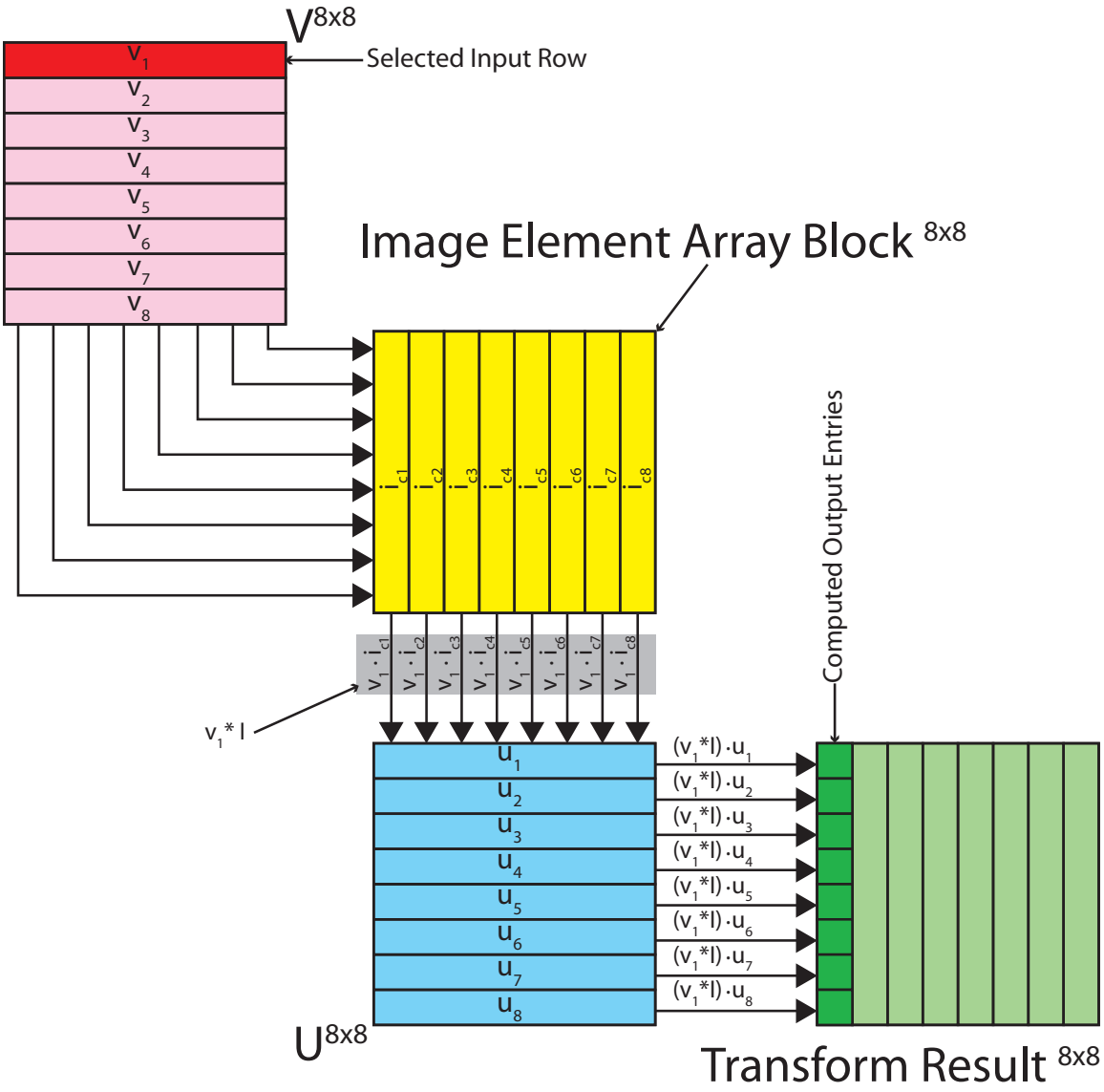


Figure 8. Matrix transform imager computational flow

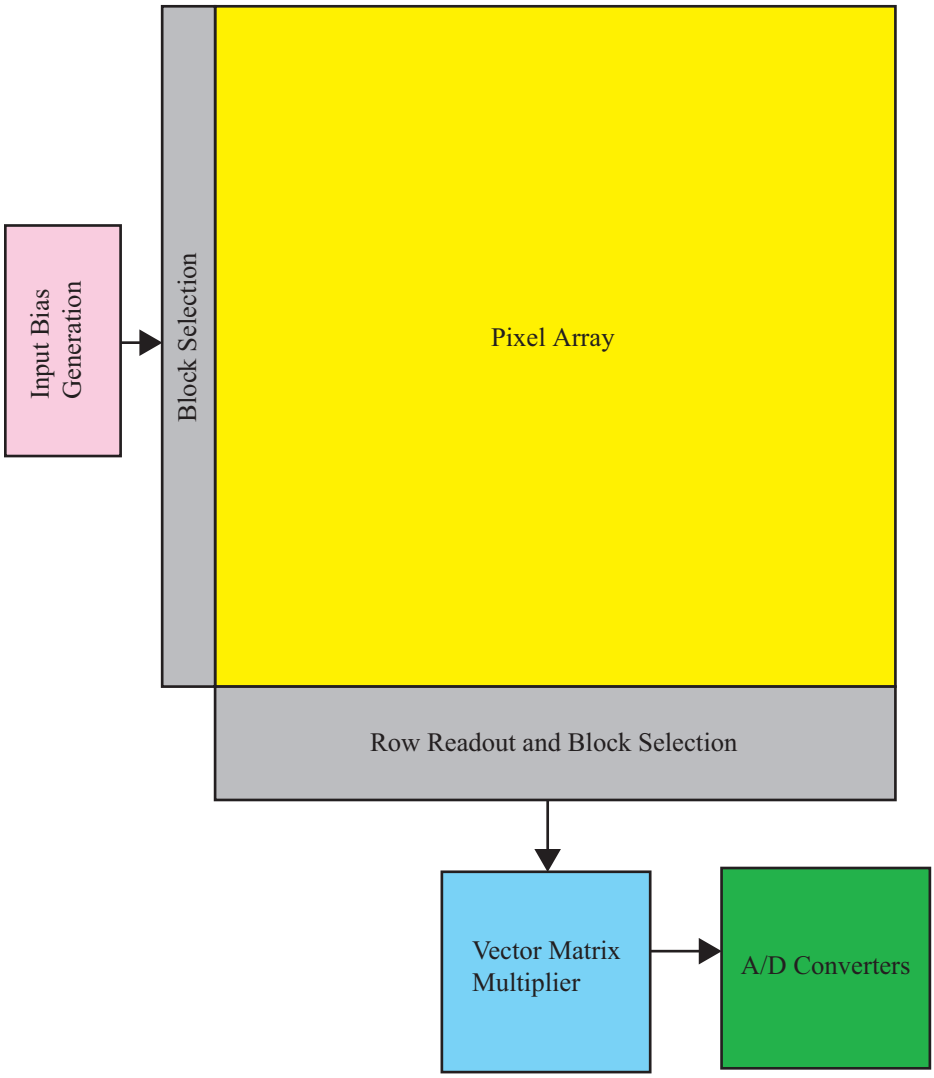


Figure 9. Matrix transform imager architecture

CHAPTER 3

PIXEL ANALYSIS

There are several sources of noise in the imager, both temporal and spacial. To remove noise from the resulting imager a better understanding of these sources and their effects had to be established. Understanding what noise effects are most prominent in the imager also help place efforts in the right places for maximum return. This chapter discusses the examination and characterization of the pixel element. First the mismatch of pixel elements is examined under the condition of uniform illumination. Then the single pixel is examined in more detail to verify its operation. Issues such as effects of shielding and verification of operation in additional sub-micron processes follow. Understanding and verifying the operation of the individual pixel and its operation in an array will be essential to later work to remove errors and enhance the imager's results.

3.1 Pixel I-V Characteristics and Mismatch

Examination of the pixel element shown in Figure 7 involves sub-threshold analysis of the differential pair since the amount of current produced by the photosensors is in the range of picoamps to nanoamps. Transistors operating in sub-threshold exhibit exponential I-V characteristics expressed in Equation 5.

$$I_D = \frac{W}{L} I_t e^{-\frac{V_t}{U_t}} e^{\frac{\kappa V_g - V_s}{U_t} - \frac{\kappa V_g - V_d}{U_t}} \tag{5}$$

A sub-threshold differential pair exhibits the relation:

$$I_{diff} = I^+ - I^- = I_{ref} \tanh\left(\frac{\kappa(V_1 - V_2)}{2U_t}\right) \tag{6}$$

Replacing the reference current with the photodiode current and taking the linear region results in:

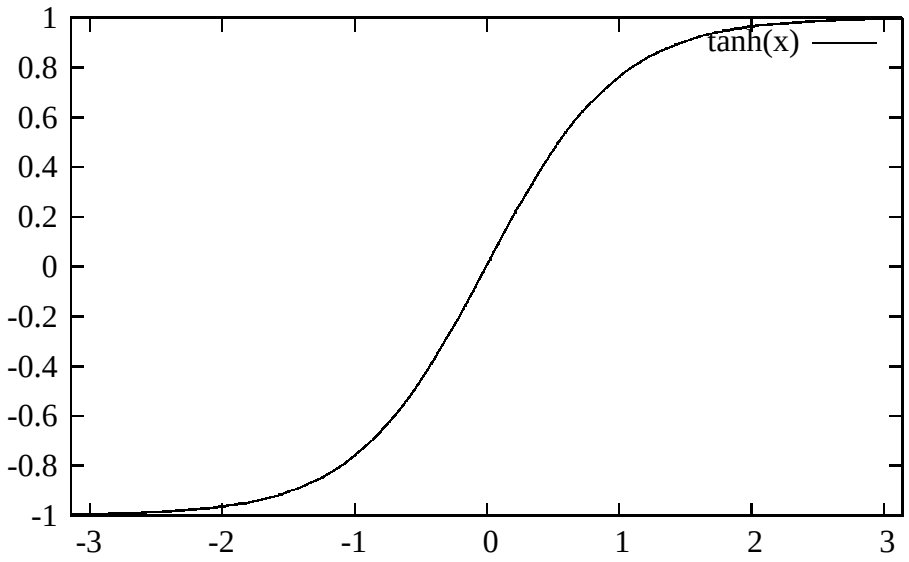


Figure 10. Hyperbolic tangent function

$$I_{diff} = I^{+} - I^{-} = I_{photo}\left(\frac{\kappa(V_1 - V_2)}{2U_t}\right) = I_{photo} * M * (V_1 - V_2) \tag{7}$$

where M is just the constant

$$M = \frac{\kappa}{2U_t} \tag{8}$$

For reference, a hyperbolic tangent curve is shown in Figure 10 since it is at the center of a lot of discussion. A brief set of characteristics of the tanh curve are that it crosses through the origin, it behaves like a linear function near zero, and it levels out to constants -1 and 1 at the respective ends.

A single I-V sweep of differential pixel in an array is shown in Figure 11. The first thing to note is that the curve in Figure 11 does not appear centered vertically at zero, but instead a point called I_{mid}. This offset is cause by a combination of factors including parasitic currents and effect of other pixels in the same column. Since the effects that cause the offset are mostly shared along a column, column striations appear in images read from the imager. Figure 12 shows these I_{mid} offsets for a two dimensional pixel array. The column

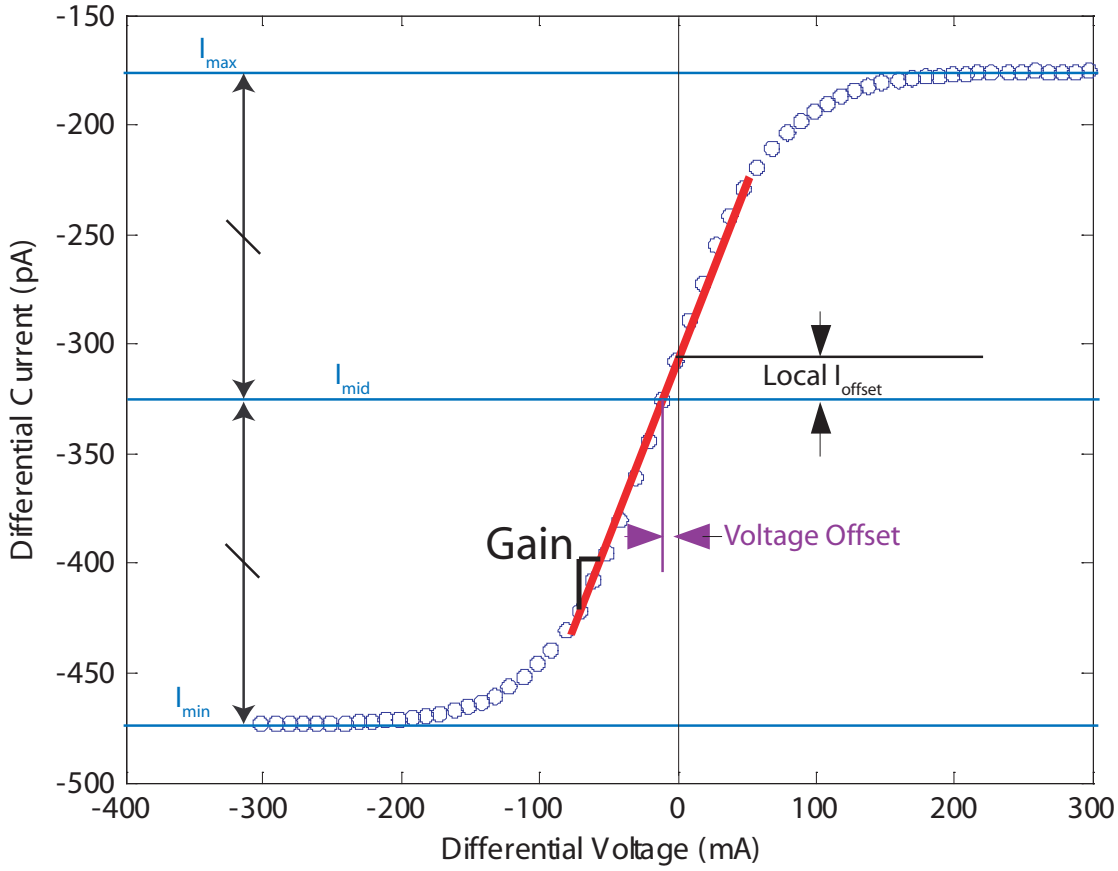


Figure 11. Typical I-V response sweeping a pixel in an array

striations are clearly visible here.

Now, if mismatches in the threshold voltages of the two transistors occur, a horizontal voltage offset of the curve results. W/L mismatches have much less of an effect then threshold voltage V_t, since V_t is exponentiated along with V_1 and V_2 while W/L is not. The voltage offset of the curve is found by taking the voltage which the I-V curve passes through I_{mid}. In this example curve, a negative voltage offset occurs. As seen in Figure 11, this negative voltage offset causes a positive differential current to occur when no differential voltage is applied, labeled as a local current offset. A local current offset is linearly proportional to the voltage offset as long as the differential pair is operated in the linear region. When measuring this pixel in an array, all other pixels in the column were given differential voltage

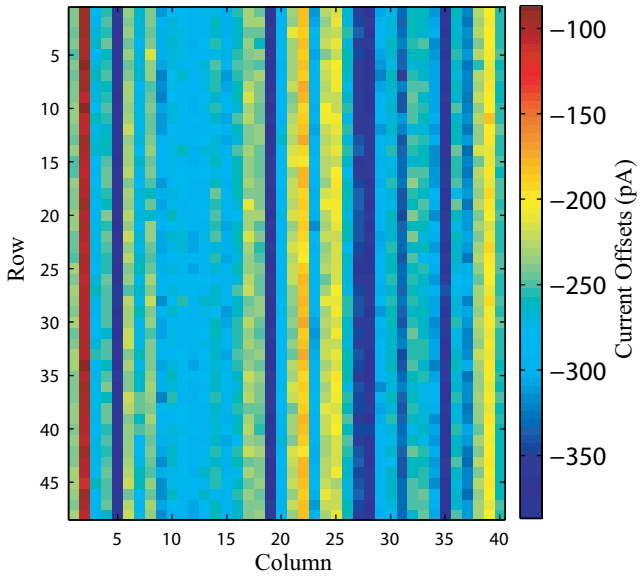


Figure 12. Current offsets showing large column striations (column offsets)

of zero. Since each of the pixels in the column has its own voltage offset, they contribute collectively to a column offset inversely proportional to the voltage offsets. This offset is partially responsible for the large current offsets of the I-V curves. This inverse correlation can be seen in Figure 13, which shows the mean voltage and current offsets for each column of a pixel array. There is not a perfect correlation since there are other factors in the column offsets.

There are several parasitic reverse biased diode junctions along the column line that exhibit leakage current. To make matters worse, these junctions are subjected to light which means that they act as parasitic photodiodes. The combination of parasitic photodiodes and the voltage offsets of each pixel contribute an image dependant offset to each column. It is image dependent because the amount of light falling on each pixel determines the contribution to the column offset. Image dependence simply means the offset will not be constant. The make removing it more difficult then just simply subtracting a constant from each column. Column offsets are faced by other CMOS imager architectures including APS imagers [8]. In APS imagers however, the column offsets have been attributed mostly to offsets in column amplifiers. Fixed pattern noise is treated as a combination of a column

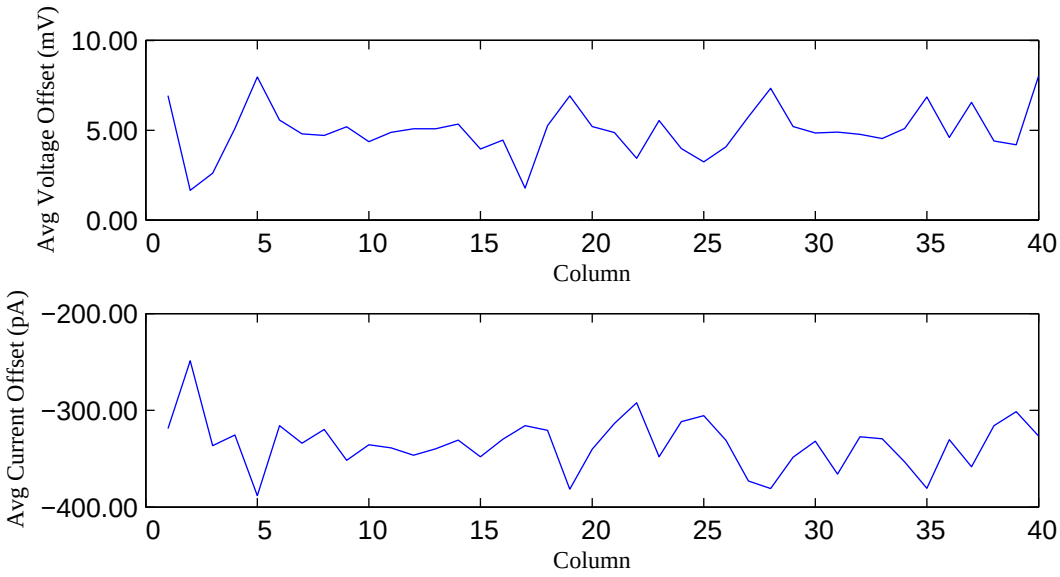


Figure 13. Average column voltage offsets and column current offsets. As expected positive voltage offsets correlate with negative current offsets.

offset and pixel offsets. Here the distinction is that the individual offsets actually create a contribution to the the column offsets. Of course the use of column readout circuitry in this differential pixel architecture will create additional offsets.

Also effecting results in the characterization chips used was voltage spike protection on the output lines. This was implemented using reverse biased diodes to power and ground. These reverse biased diodes unfortunately act as large photodiodes. To reduce the effects of the diode protection, later characterization chips moved the diode protection away from the edge of the chip so that they could be shielded from light better.

The next parameter of the tanh curve to be discussed will be gain in the linear region denote by a red line in Figure 11. Gain is defined as the change in differential current vs. change in the differential voltage, also called transconductance. From Equation 7we see that the gain term is simply

$$Gain = I_{photo} * M \tag{9}$$

Rewriting the output current to exemplify the effect of the gain term gives

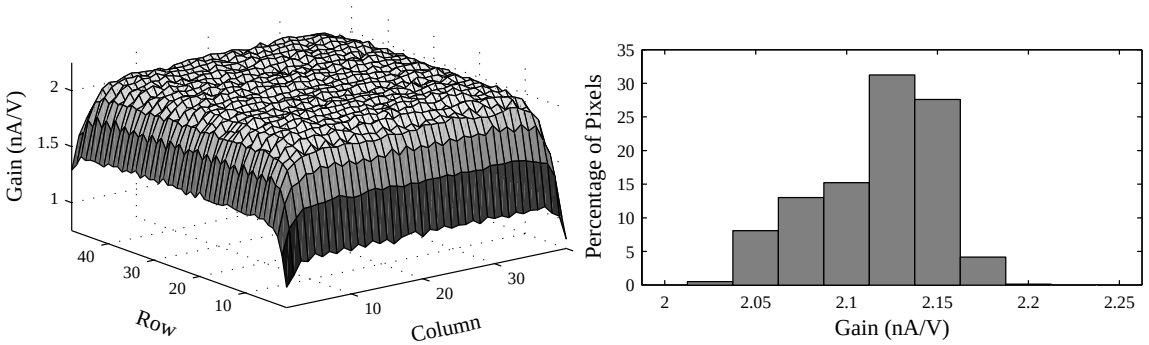


Figure 14. Gain mismatch. (a)Gain as a function of pixel position. (b)Histogram of gains (outer 8 pixels are excluded from statistics)

$$I_{diff} = Gain * Vdiff \tag{10}$$

Gain can also be written as

$$Gain = I_{photo}\frac{\kappa}{2U_t} \tag{11}$$

with units become A/V.

Also note that kappa can be solved for using

$$\kappa = Gain * \frac{2U_t}{I_{photo}} \tag{12}$$

I_{photo} can be found experimentally by using the fact that the height of the tanh curve is $2 * I_{photo}$. Taking the difference of the two extremities of the tanh curve gives us this value needed to solve for $kappa$.

To measure these parameters over an array of pixels, individual I-V sweeps were taken. The extracted parameters are shown in Figures 14,15,16, 17. Again, the current offset was found by finding the middle current of each pixel, previously referred to as I_{mid}.

These measurements were taken slowly through an ammeter over the course of several hours with averaging to reduce measurement errors. The extracted values depended on the accuracy of the measurements which were very small currents. Measuring small currents

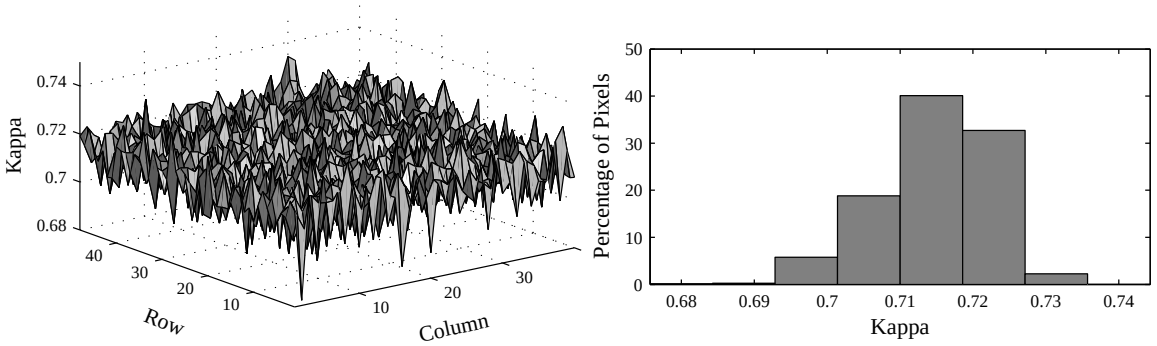


Figure 15. Kappa mismatch. (a)Kappa as a function of pixel position. (b)Histogram of kappa

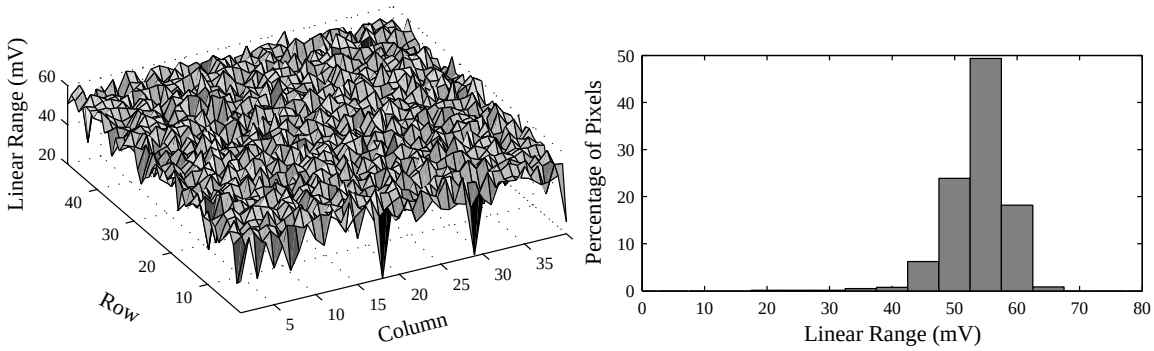


Figure 16. Linear range. (a)Linear Range as a function of pixel position. (b)Histogram of linear ranges

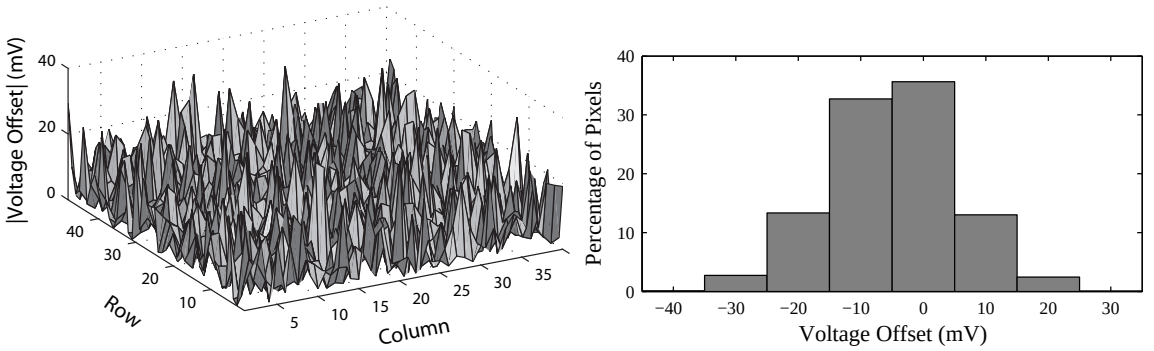


Figure 17. Voltage offsets. (a)Absolute voltage offsets of differential pairs as a function of pixel position. (b)Histogram of voltage offsets

Table 1. Statistics extracted from the pixel array

	Mean	Std. Dev.
Gain	2117.4pA/V	33.6pA/V
Linear Range	54.4mV	4.3mV
V_{offset}	4.9mV	10.0mV
$\lvert V_{offset} \rvert$	8.9mV	6.7mV
Kappa	0.715	0.007

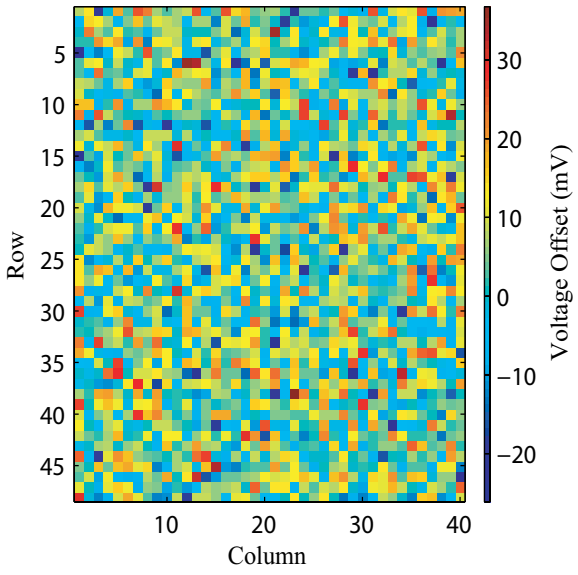


Figure 18. Voltage as a function of position, showing a mostly random distribution of voltage offset. Spacial random effects dominate any gradients that may be present

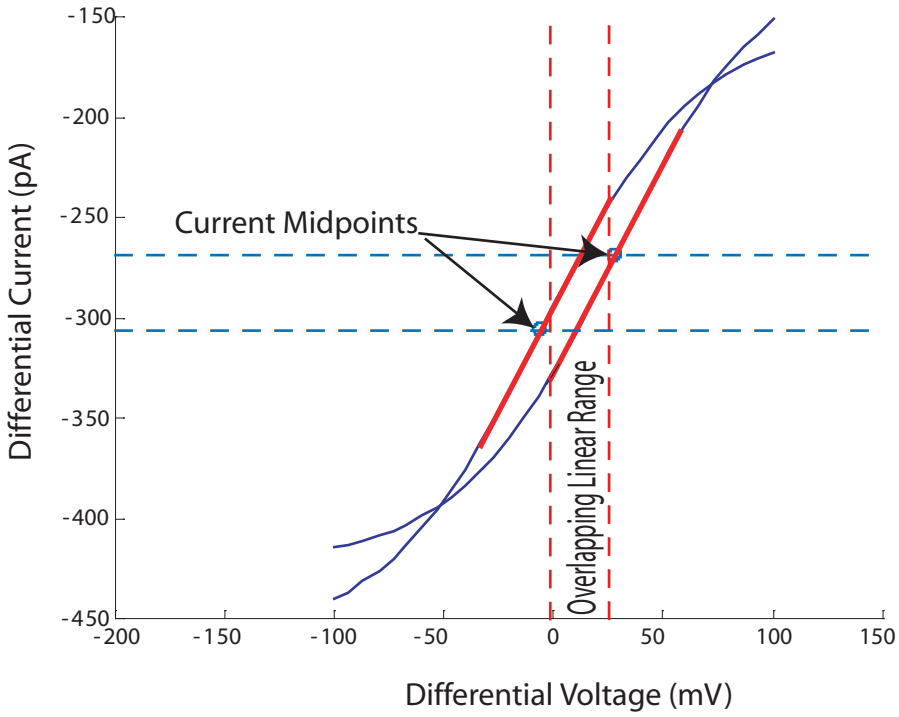
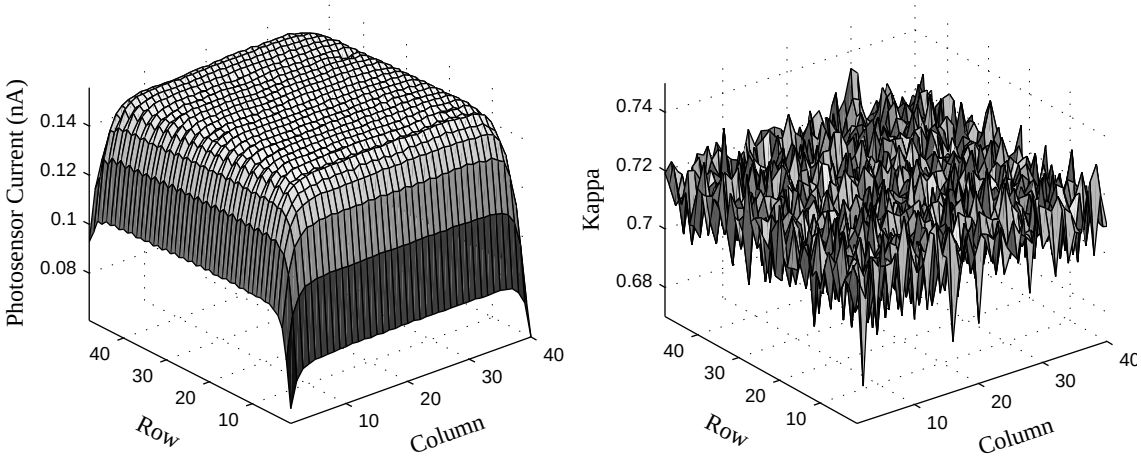
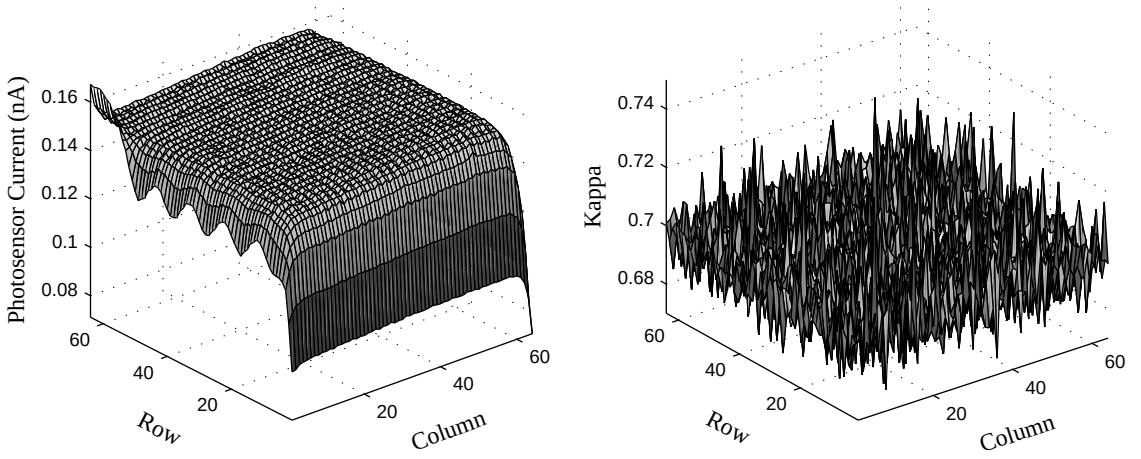


Figure 19. Overlapping linear ranges. Since multiple pixels are used at once, input voltages must fall within the linear range off all pixels used. Voltage offsets reduce the overlapping linear range available.



(a)



(b)

Figure 20. Edge effects of two different imager layouts, (a) and (b), with the same pixel design but different peripheral circuitry.

off chip is noisy by nature. Even small moments of people in the surrounding area can cause misreads that affect the data. Reading these current using on chip structures would definitely be preferable if they could be properly calibrated. Any future work would definitely benefit from an on chip measurement approach. For instance, the extracted gain standard deviation where affected by measurement noise. Even though the absolute accuracy of the numbers may not be known, the data still shows trends of interest. They give the desired indication of where mismatch will effect performance and what mismatch can be compensated.

Figure 14 shows the gain across an array under nearly uniform illumination. Edges effects characteristic of CMOS imagers are clearly seen as in other array characterizations[9]. Since pixels near the edge of the array have different surrounding then the pixels toward the middle, they tend to vary. The gain mismatch seems to originate from variation in the photodetector current as seen in Figure 20. The edge effect does not always show a falloff, and different edges on the same imager may show different characteristics. Edge effects did seem consistent on chips on the same process run of the same design. The edge effects also seemed to be more prominent on edges next to other circuitry such as decoders. These edges may have also been effected by the distance of a p+ grounding guard ring from each edge, which is placed around the pixel array and analog circuitry. It would have a close proximity to the array at edges without circuitry. Off axis lighting was also suspected since on two edges light may be blocked by the shielding whereas the at other two edges the light would be allowed light to slip underneath the shielding. A variation of lighting angle showed a variation in currents at the edges as expected but the underlying edge effects were still consistent. There seems to be no edge effects in the kappa measurements, again suggesting that the effect occurs in the photodiode itself and not the transistors. So the gain error is caused by mismatch of photosensor size and efficiency and also kappa. Overall though the gained seemed to be within usable margins of error.

Moving to voltage offset measurements, the results in Figure 17 and Figure 18 show

voltage variations mostly all in a $\pm 30mV$ range as expected. A normal distribution slightly offset from zero resulted. The main concern arising from these measurements for voltage offset is its effect on the effective linear range of operation along a row of pixels. Since a voltage input is applied along a row, it must be in the linear range of every pixel being used at once on that row. Figure 19 shows how even two pixels with individual voltage offsets have a reduced overlapping linear input range. If these offsets become too large compared to the linear ranges of the pixels, Figure 16, then special treatment may be needed for these pixels. Since these pixels are outliers in terms of behavior, they do not necessarily represent an unrecoverable source of error. Schemes for adjusting voltage inputs to take full advantage of the voltage range of the pixels in use at a given time may help. If certain pixels don't allow use will the other pixels then some peripheral compensation circuitry could possibly be used.

3.2 Light levels

The assumption of the pixel's usage is that the differential current output of the pixel is a multiplication of the light intensity falling on the pixel by a differential voltage, with an added constant multiplier $\frac{\kappa}{2U_t}$. This assumes that the current through the photodiode and thus the height of the resulting tanh curve indeed scales linearly with light. It is also expected that the slope in the linear region does the same. Since the slope is also effected by other parameters, namely kappa, it may not maintain its linear relationship to voltage and light. Since kappa has certain dependencies, such as source voltage, it could alter the linear multiplication. Figure 21 (a) shows several I-V sweeps done at varying light intensities. The light intensity was controlled using light absorption filters with know transmission levels. Transmission is meant here to be the percentage of light passing through the filter. The lowest light level was produced using a transmission level of 1% while the highest level, 100%, was obtained using no filter at all. Therefore, the range of light intensities varied by two orders of magnitude. Since the pixel was in an array it had associated current

offsets which also move with light intensity. Figure 21 (b) show the same curves with there offsets removed. The offset is taken to be the average of the currents at the two extremities of the curves. To isolate the effect of the constant multiplier $\frac{\kappa}{2U_t}$ the height of the curves was normalized and the results are shown in Figure 21 (c). Smaller or larger values for κ would cause corresponding changes in the slopes in Figure 21 (c).

To also validate the linearity of the output with respect to light, Figure 22 (a) shows the tail current extracted from the height of the curves as a function of light intensity. The linear relation holds as expected. The offsets of the curves in Figure 21 (a) are plotted in Figure 22 (b). This linear relationship was also expected since sources of the error, parasitic junctions and other pixels in the column, produce currents proportional to the light intensity. Figure 23 shows how the slope of the linear region scales appropriately with light intensity. These results help validate the proper multiplication operation of the pixel.

3.3 Shielding and Light Spreading

To measure spreading effects and to observe effects of metal shielding, a chip was fabricated with four variations of metal covering. Figure 24 (c) shows a standard 18x18 array with standard metal shielding between photodiodes, covering the transistors in the pixels. Figure 24 (b) is the same layout as (c) but eliminates the metal shielding. Eliminating the shielding causes higher current levels in the photodiodes. This is expected since even light falling tin the “dead” region of the pixel will refract and be picked up by the photosensor. This same effect is shown in [6]. The alternating pattern along rows in Figure 24 is likely due to the fact that the layout of the pixel is such that the layouts of pixels are reflections of adjacent pixels for more compact layout. So, some routing occurs between every other pixel. For another comparison, Figure 24 (d) shows light falling on an array which has one pixel in the center which has standard shielding while all other pixels are completely shielded. The metal shielding has an obvious effect here, blocking most light to the shielded pixels. Here a spreading effect can be seen. Figure 25 shows the same plot with a normalized log scale

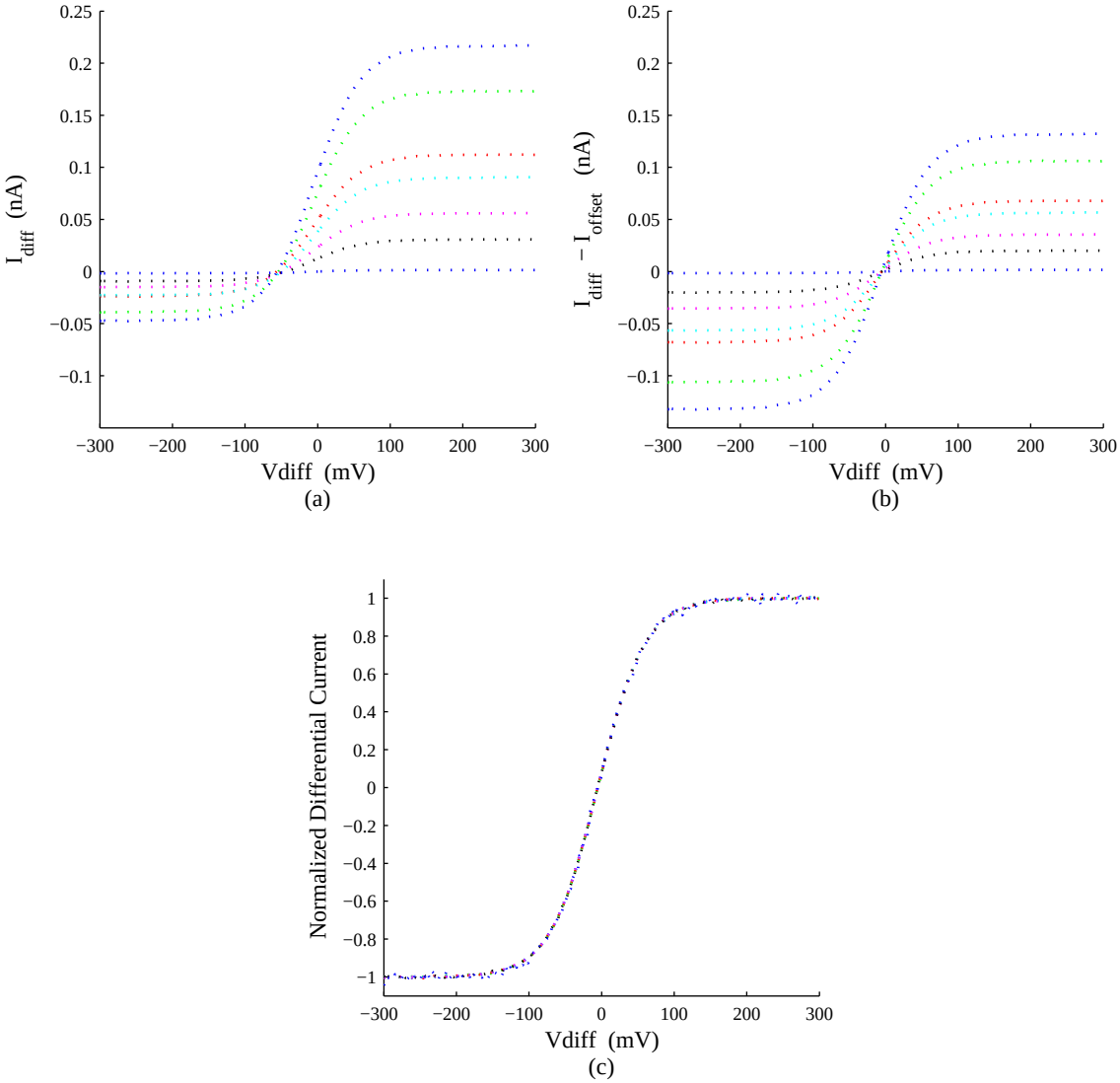


Figure 21. Pixel Currents with varying intensity. These plots show output current vs. differential input voltage for seven light intensities that vary by up to a factor of 100 from the lowest to highest intensity using light absorption filters. (a) shows the original data; (b) shows the same curves with there offsets independently removed; (c) shows the same seven curves normalized. The last plot shows the consistency of the shape under varying light intensities. This verifies that the slope in the center scales with the height of the curve and that κ stays constant.

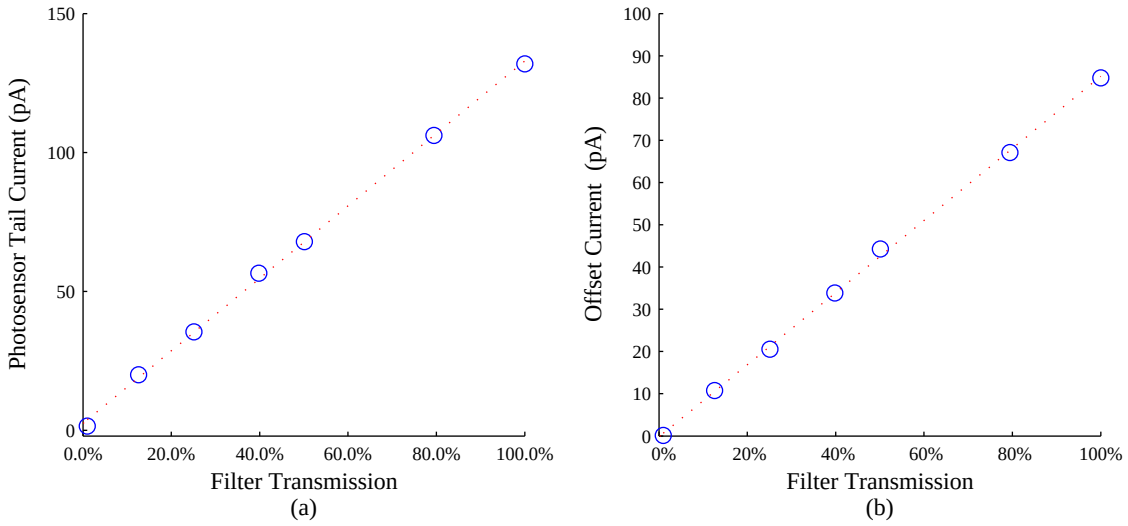


Figure 22. Photosensor tail current as a function of light intensity controlled using light absorption filters. (a) shows that the photosensor current feeding the differential pair is linearly proportional to the light intensity. (b) shows that the offset of the curve is also linearly proportional.

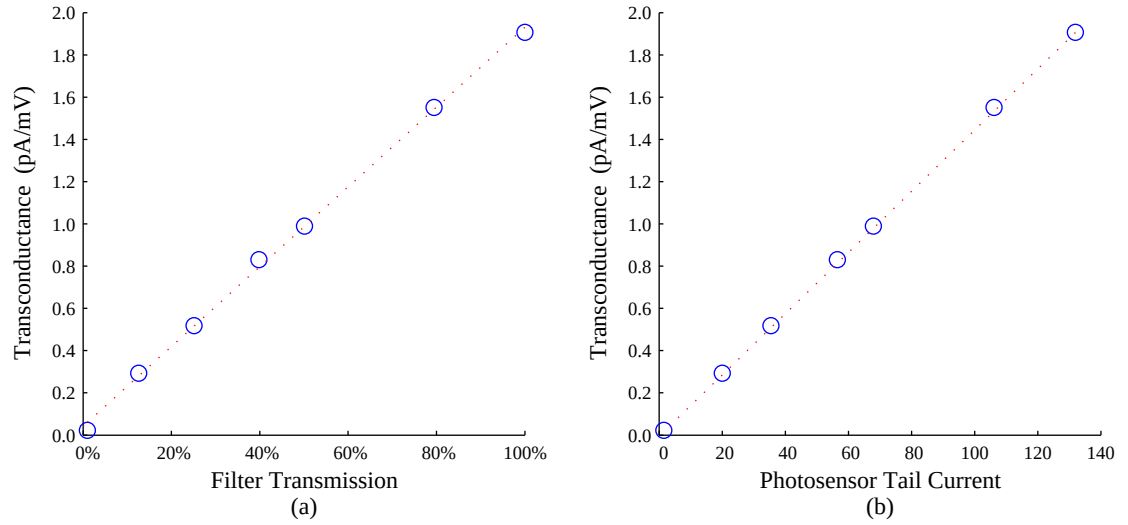


Figure 23. The transconductance of the differential amplifier as related to light and saturation current.

to better view the spreading effect. It shows an obvious effect even 3 pixels away. It is also obvious that the center pixel has a reduced current since it is surrounded by shielded pixels which don't share any light. For a final comparison, Figure 24 (a) has an entire column of normally shielded pixels with the remaining being completely shielded. Again, its current levels along the column are larger then the single pixel in Figure 24 (d) since each pixel receives contributions from neighbouring pixels. An initial guess would be that a convolution of the the spreading in (d) could produce (a) but this effort was not immediately successful. Further investigation may prove useful in revealing a compensation method for spreading. These spreading issues become especially important in applications where large light variations occur in a small locality such as star tracking [6] and other target tracking.

3.4 Variation of Common Mode Voltage

Figure 26 shows the relation of differential current and differential voltage when different common mode voltages are used. As the common mode of the differential pair is increased, the source voltages are pulled up. Since the voltage on the photodiode is greater the current is increased. Higher source voltages also increase the depletion width so that the depletion capacitance decreases and kappa increases. Figure 27 shows the same curves with the heights normalized, canceling the effect of the curves height on the slope in the linear region. Unlike the normalized curves in Figure 21 (c), the changing slopes of these curves show a change in kappa.

The pixel even works with a common mode of 0 volts since the photodiode can actually pull the sources of the NFETs below ground. At this point though the diode does start to exhibit behavior much different then when a it has a larger forward bias on it. It become much more sensitive to voltage changes since the diode begins to shut off in this region.

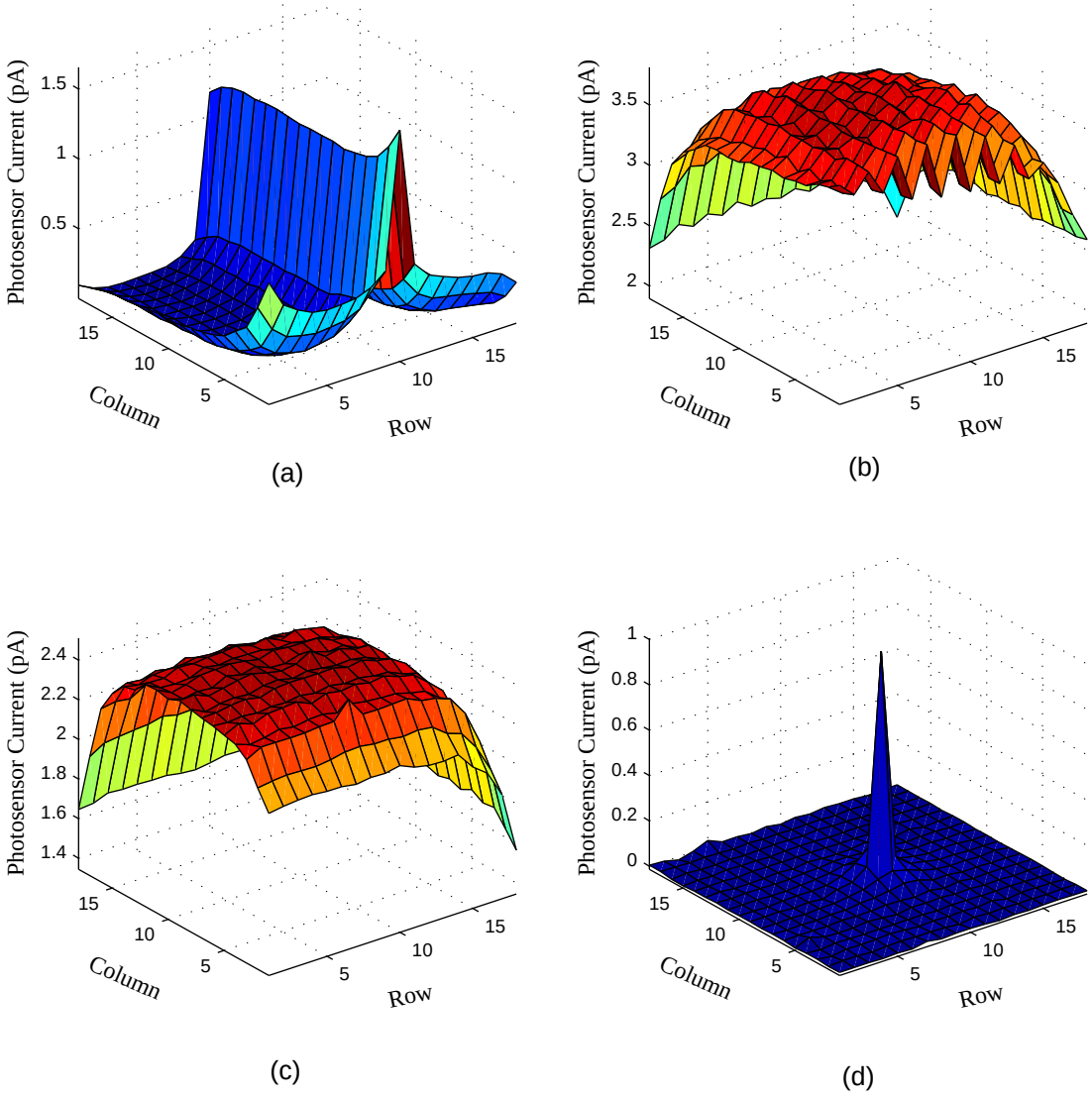


Figure 24. Results from various metal shield coverings. (a) shows a pixel array completely shielded except for one column. (b) shows an array with no shielding. (c) shows an array with proper shielding of transistors. (d) has all pixels shielded expect for the center pixel, showing a spread effect

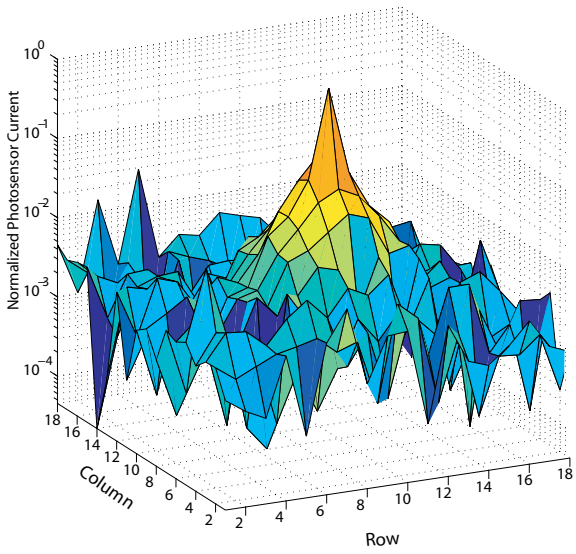


Figure 25. Logarithm of normalized light spreading. The maximum current was normalized to 1.

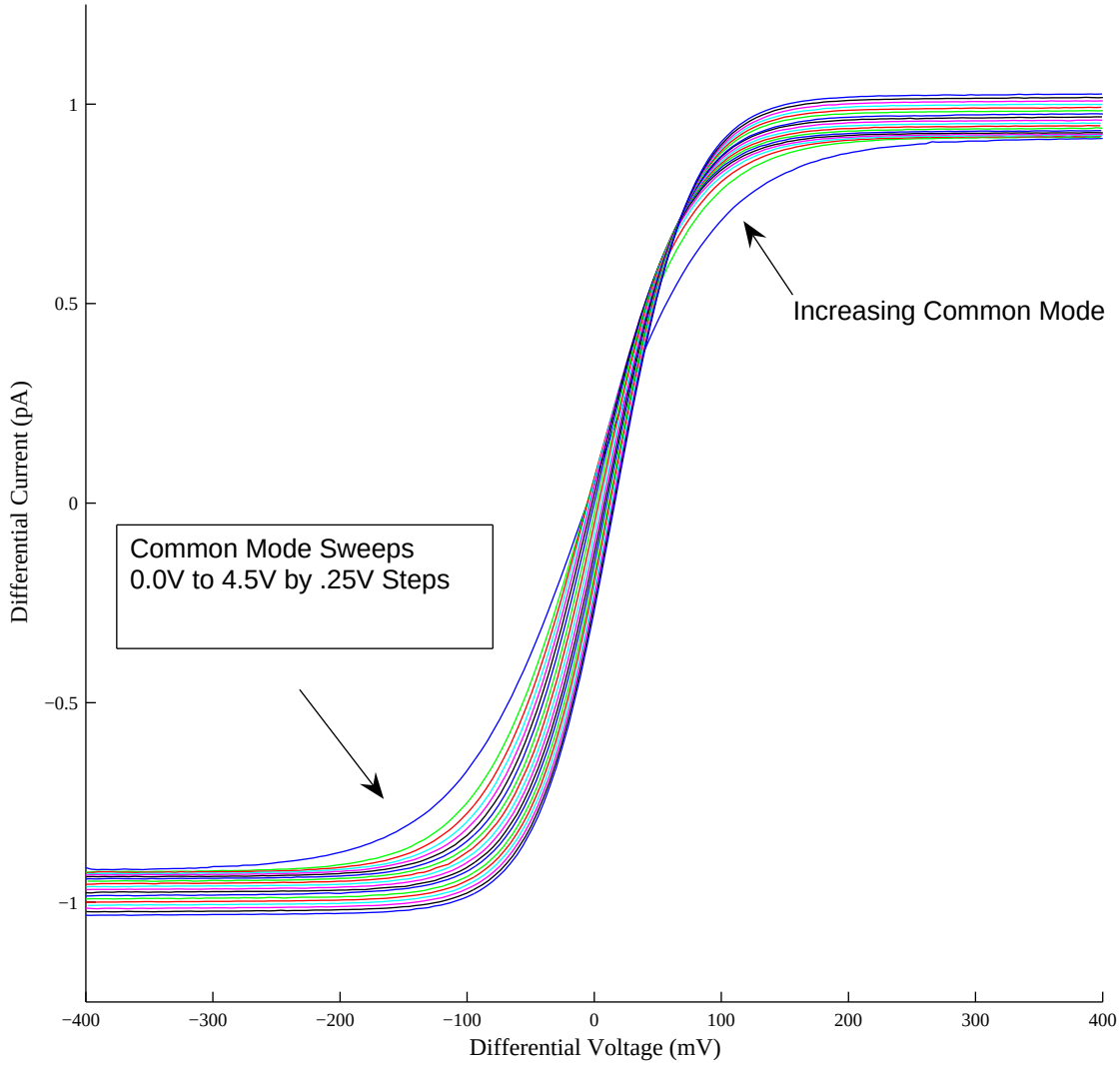


Figure 26. I-V sweeps with varying common mode voltage showing the increase in pixel current and gain in the linear region. The pixel operates even at a common mode of zero volts since the photodiode can pull the source voltage below ground.

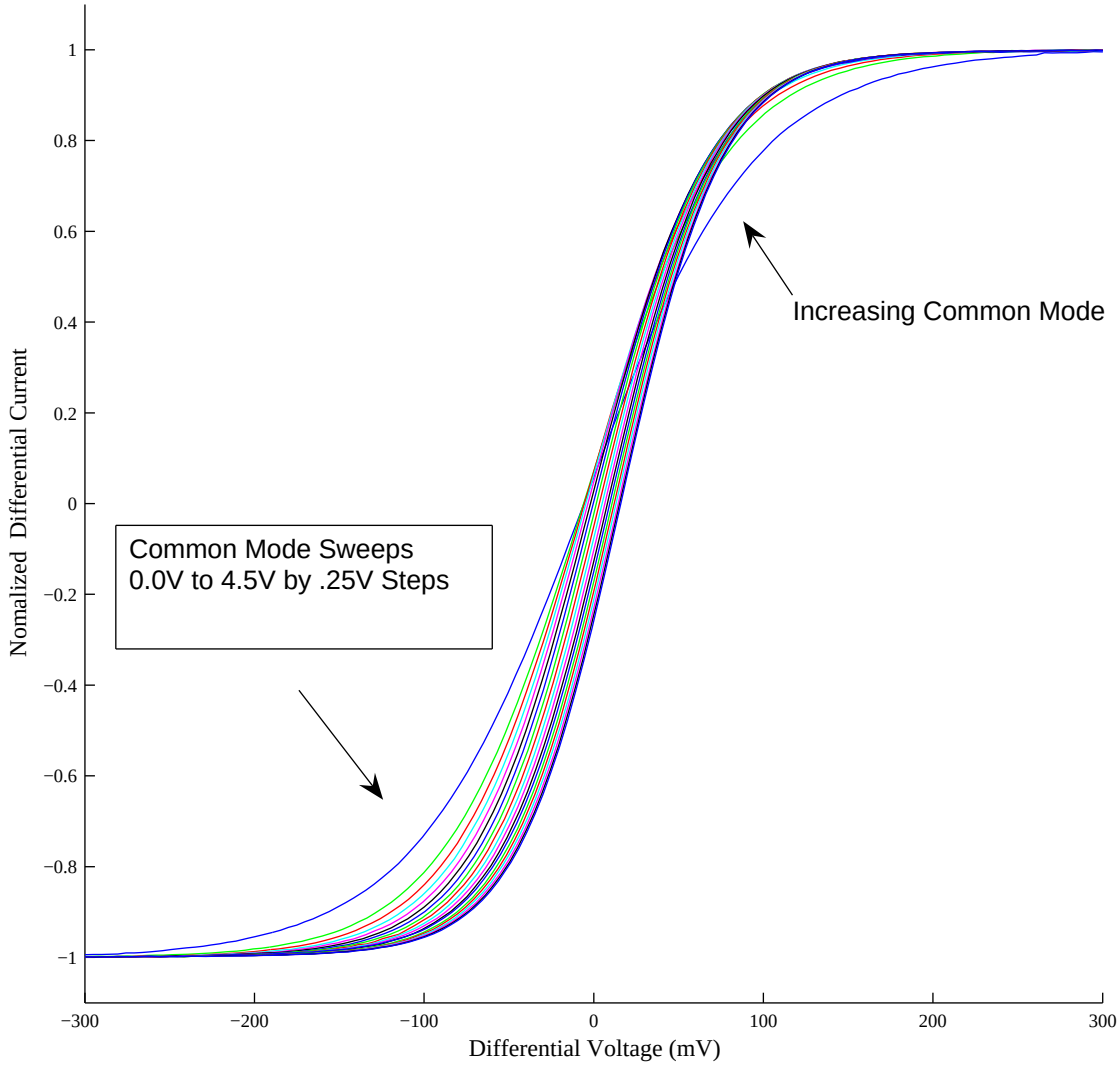


Figure 27. Normalized I-V sweeps with varying common mode voltage. Normalizing removes the effect of the height of the curve on the slope in the center. The variance here shows that kappa increases with high common mode.

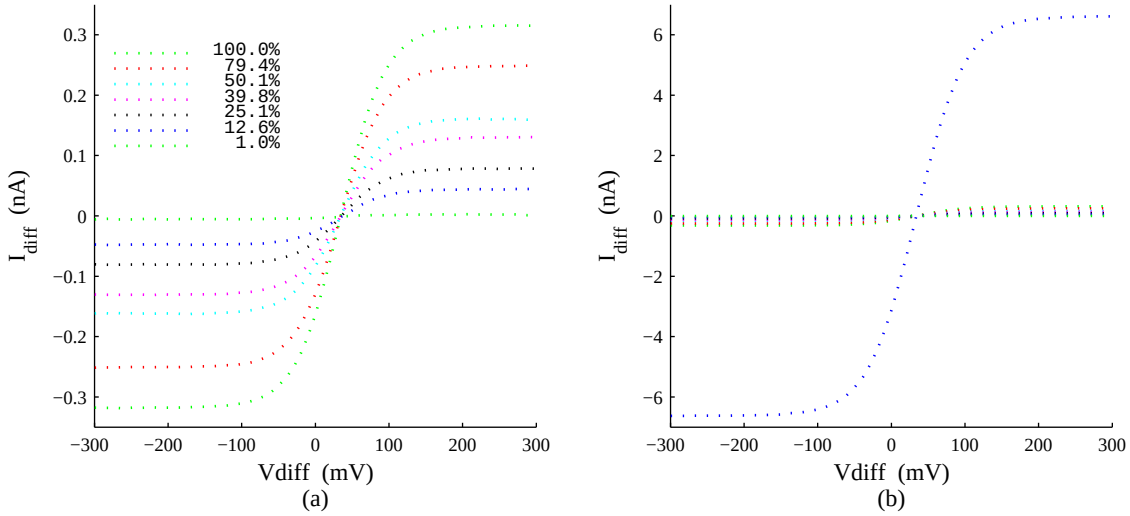


Figure 28. Light Intensity sweeps on a .18μm process. (a) shows several curves taken under varying light intensities using light absorption filters so that there relative intensities are known.(b) shows the same seven curves plus an additional curve with a much higher light intensity.

3.5 Verification of Operation in Smaller Processes

Though one of CMOS imagers' strongest points is the ability to be fabricated using standard processes, a designer does not has any specifications or guarantees for operation in a particular process. This leads to the need for prototyping a photosensor application. This differential pixel structure was therefore fabricated on a .35μm process and a .18μm process. The operation of these pixel structures was then verified.

Figure 28 (a) shows the I-V sweeps taken under light intensities varying in two orders of magnitude. To push this experiment further the light intensity was increased, but without known relative intensity to the other curves. Figure 28 (b) shows the same curves in (a), but with an additional I-V sweep taken under higher light intensity. The curves were then normalized as shown in Figure 28 (b) showing that the gain in the linear region of the curve is approximately linearly proportional to light intensity and photosensor current over several orders of magnitude of light. Figure 30 shows the expected linear relation of light and photosensor tail current. Gains extracted from the linear region of the curves are shown in Figure 31. Figure 31 (a) shows the data points taken from the known light intensities

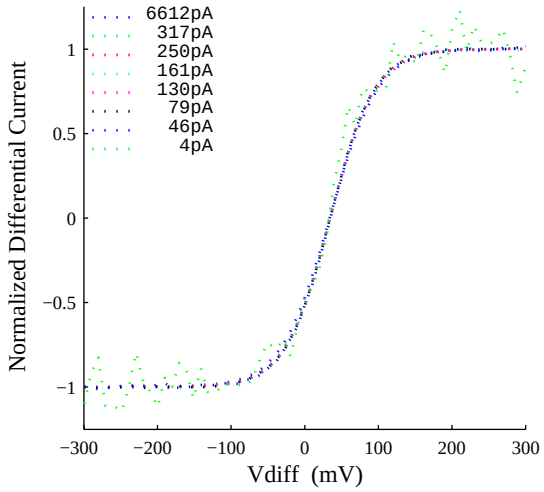


Figure 29. Normalized curves at various light intensities, from a .18μm process

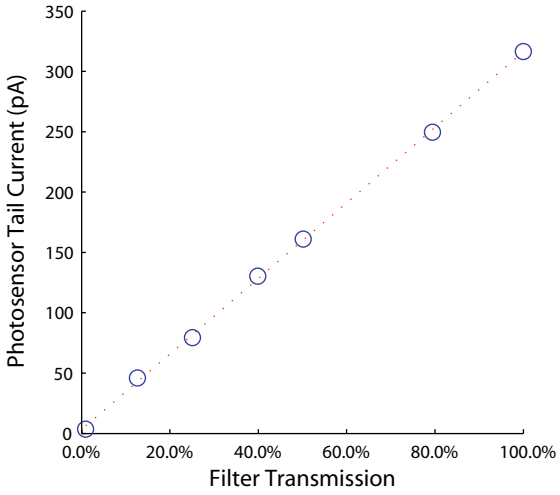


Figure 30. Light intensity versus tail current on a .18μm process pixel

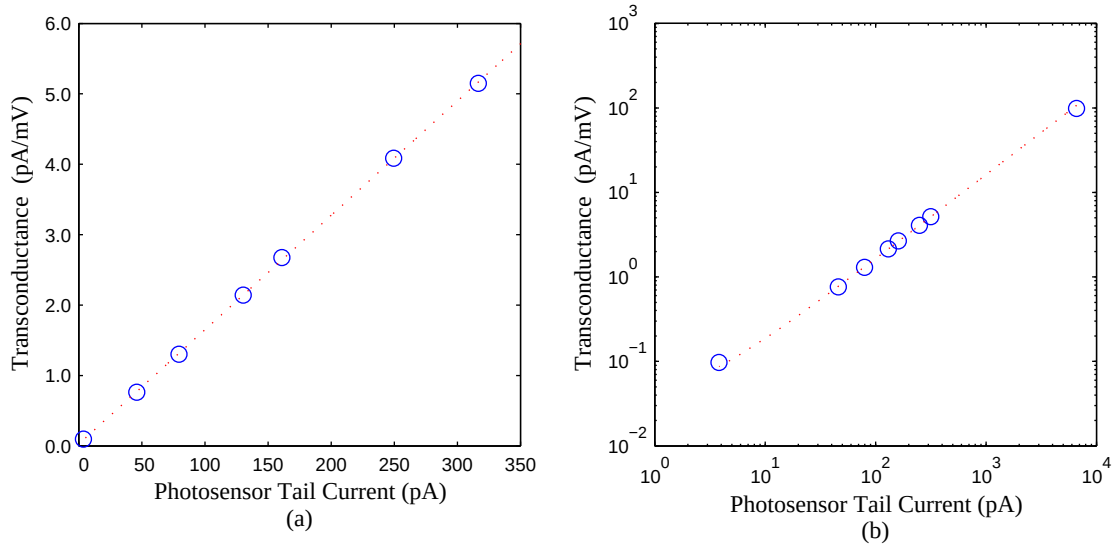


Figure 31. The transconductance of the differential amplifier as related to light and saturation current. Pixel is is on a .18μm process (The middle 6 points are used for the line fit)

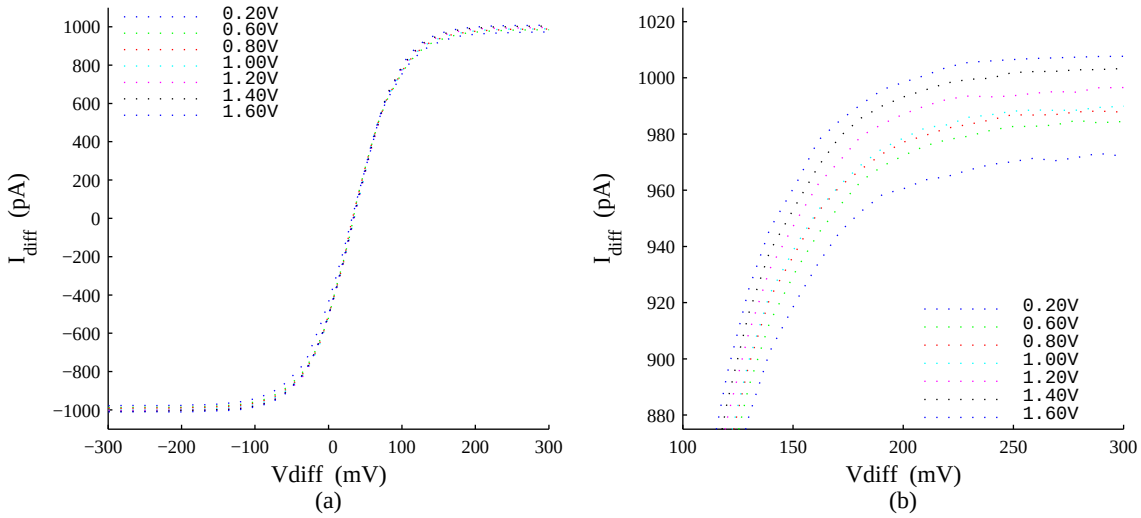


Figure 32. Several I-V sweeps taken at various common mode voltages. Pixel is on a .18μmprocess

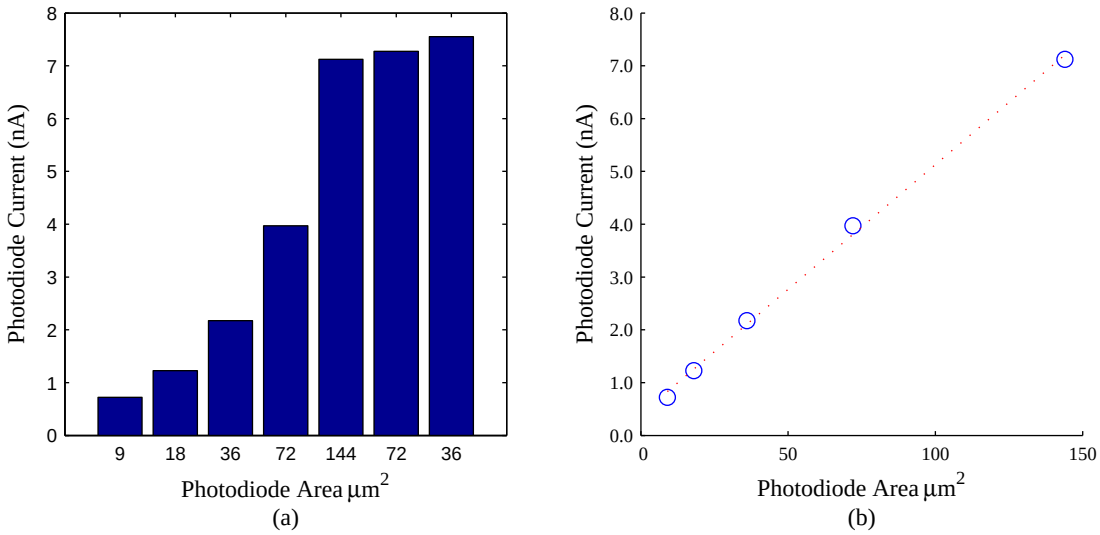


Figure 33. Size of pixel vs current on .18 process. The last three values in (a) are taken from pixels of the same size but with various portions covered by metal. The metal shielding has little effect here.

while (b) shows the additional data point taken, which is about three and a half orders of magnitude greater current. This chip was operated at about 1.8V. As Figure 32 shows the structure is flexible enough to be operated with a range of common mode voltages. Here proper operation is obtained even when voltages on the pixels are less then 50mV. Figure 32 (b) shows a zoomed view of a section of (a), revealing the expected increase in photosensor current larger common modes. Larger common mode voltages pull the voltage on the photodiode up, which results in increased current since the photodiode is not a perfect current source.

Also a factor in pixel current is of course the size of the pixels. An array of pixels sizes was exposed to a roughly uniform light source and as expected the light scales with the size of the pixels.Figure 33 (b) shows this relationship. To also bring into question the effectiveness of metal shielding, the last three values in Figure 33 (a) show the same pixel size with various portions shielded by a third level metal covering. The metal shielding here, unlike the previous .5μm process, does not seem to have an effect. Unfortunately, these chips seems to be very susceptible to failure during usage compared to .5μm chips used previously. Though voltage protection was used on inputs gates, several chips suffered

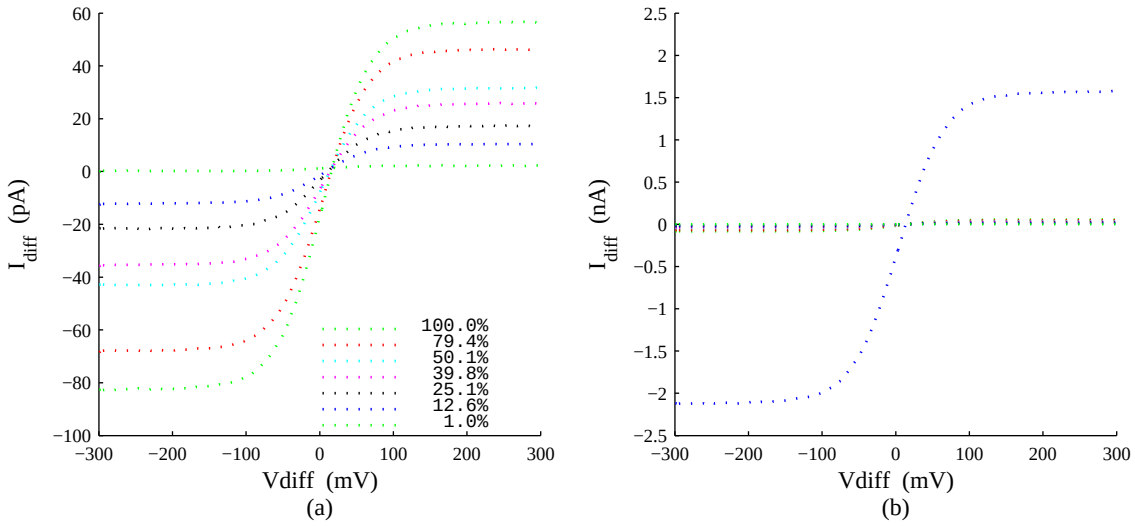


Figure 34. Several I-V relations taken on a .35μm process at various light intensities. (a) shows curves generated using light filter (b) shows the same curves plus additional curve at a much brighter intensity.

permanent damage during usage until a low-pass R-C circuit was used to filter the voltage inputs. The inputs were from a noisy source and the small oxide size of this process may be less resistant to damage during momentary spikes.

Many of these verifications were repeated for a .35μm process. The notable difference here was much lower currents. While the .18μm chips produced reasonable current levels comparable to the .5μm chips, these .35μm chips had current levels in the tens of picoamps. This can most likely be attributed to a salicide layer on this processes which implants the active regions with metal to reduce active resistance. While desirable for most designers, CMOS imaging does not benefit from a coat of metal painted on top of the photodiodes, which are just an active region in a substrate or well. Even at these lower currents, the pixel operated much as expected over several orders of magnitude of light. Since these chip were a little more rugged, more enough data in the curves was collect to extract values for κ. For the middle six data points, a value of 0.814 for κ was obtained.

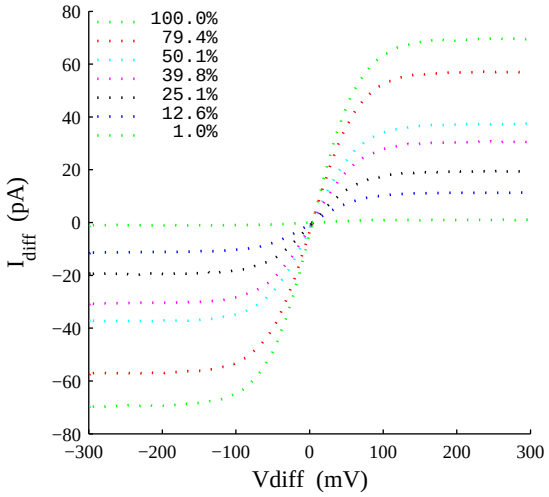


Figure 35. Centered filter curves from various light intensities on a .35μm process

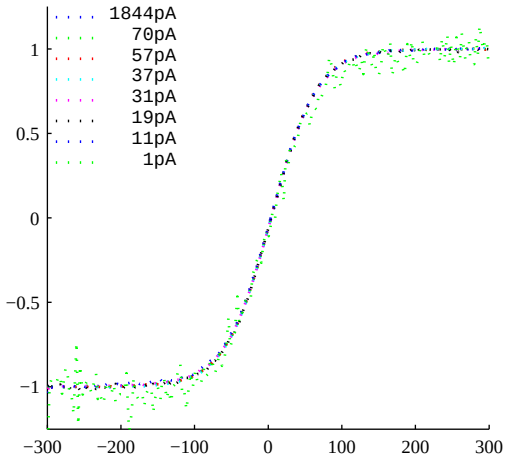


Figure 36. Normalized filter curves from various light intensities on a .35μm process shows little change in kappa over varying light intensities.

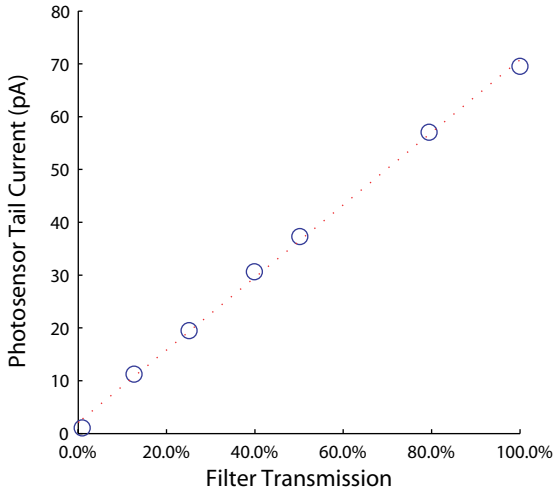


Figure 37. Light intensity versus tail current on a .35μm process pixel

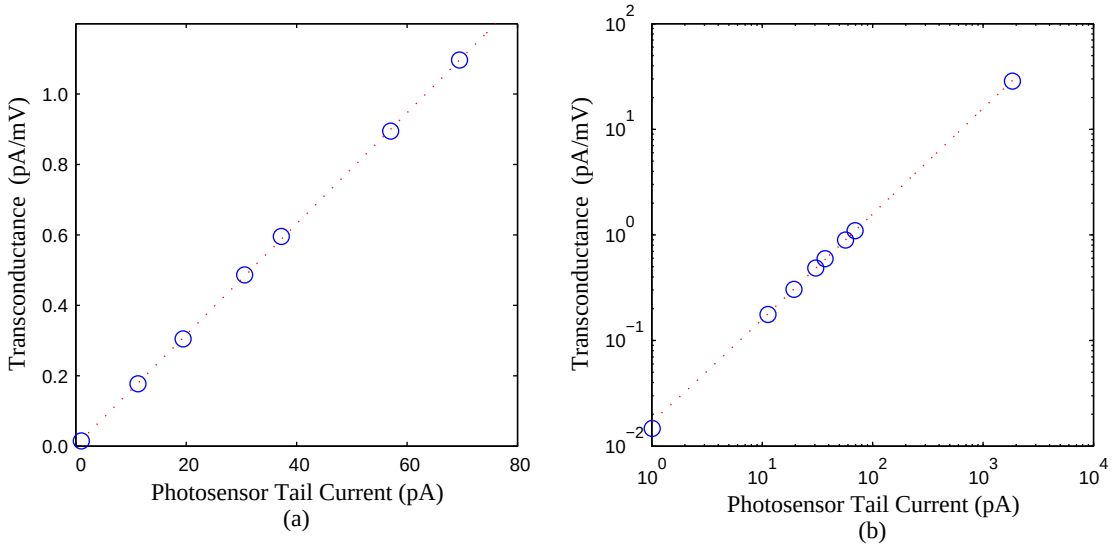


Figure 38. Transconductance vs light induced current in .35μm process pixel. (a) shows points collected from light filters while (b) includes extra point from much brighter light

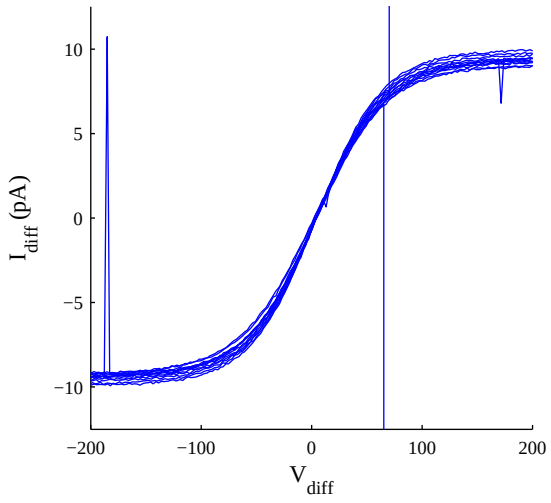


Figure 39. Several I-V sweeps taken at various common mode voltages from 0.25V to 3V stepping by .25V. This shows and wide range of operational choices for common mode voltage.

3.6 Layout Considerations

Under a uniform illumination, all pixels should ideally produce the same amount current. In some chips, under a mostly uniform illumination, a small but noticeable spacial pattern existed in the currents extracted. These tail current are essentially a representation of the image captured by the imager. This image is seen in Figure 40 (a). An examination of the image in the frequency domain, Figure 40 (b), pointed out some obvious unwanted components. The two dimensional FFT reveals a lot of energy in the horizontal DC components, seen in the first row of the FFT. The FFT also reveals a lot of energy in the highest frequencies. The highest frequencies in an FFT correspond to a spacial period of two pixels. This means that a pattern occurs that repeats every other pixel. The first suspected culprit for this is the fact the the layout involves a lot of mirroring between every other pixel. This is done to save area, increase fill factor, and increase spacial resolution. But if better spacial resolution will not provide enough additional information to compensate for the loss of information due to the offsets, then the mirroring needs to be avoided in favor of uniform layout with better matching.

To further examine effects of alternating pixel layouts a chip was fabricated and tested which had four different layouts. Figure 42 shows the layout schemes tested. In each differential pair the positive and negative transistor is respectively define by its gate connection to voltage V^+ or V^-. These gate connections are highlighted by the color red. In the vertical direction purple current lines are labeled I^+ or I^- to show the ordering along a row. A full pixel array can be made by laying out out a group of four pixels and tilling it. The group of four pixels can be simply a tiling of a single pixel layout, as shown in quadrants (a) and (d) of Figure 42. Alternatively, for a group of four pixels, the left two can be the same and then mirrored to form the right two. This creates an imager array where every other column is flipped horizontally. Such a layout pairs up positive transistors and negative transistors along a row so that ever pair can share a single polysilicon line. Sharing polysilicon means

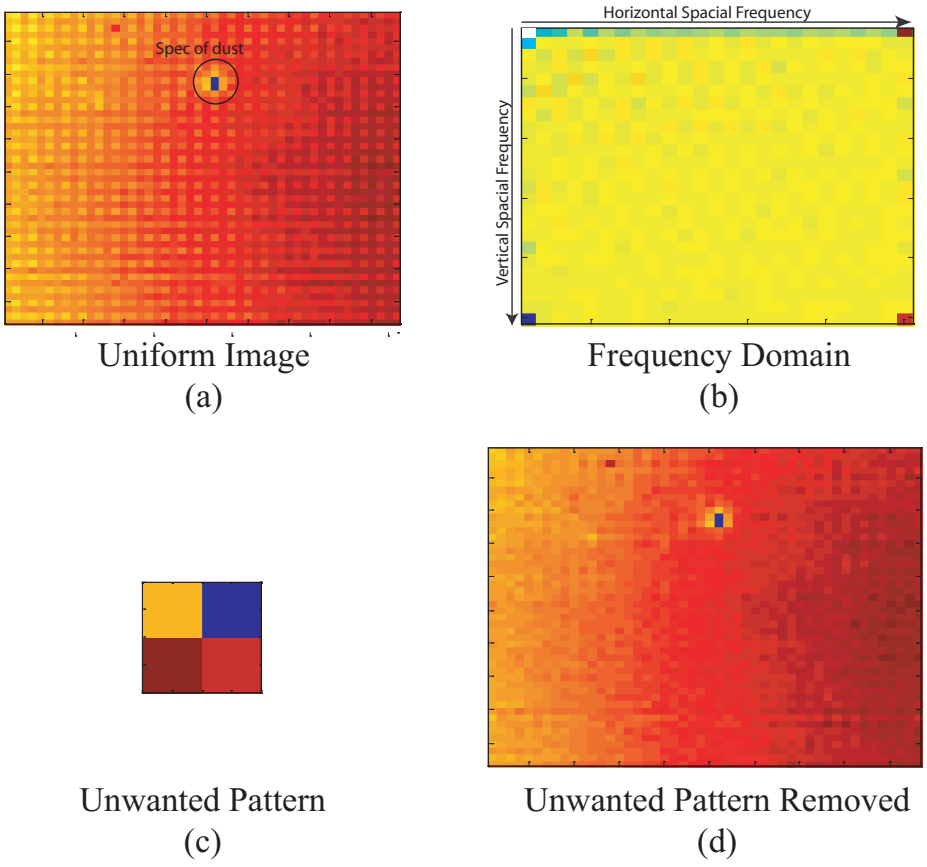


Figure 40. Error patterns. (a) shows extracted currents from the pixel array under a fairly uniform illumination. The gradient seen is due to slight variance in the light. In the frequency domain (b), there are unwanted components in the highest frequencies corners. These creates a spacial pattern (c) which when removed results in (d).

less metal to poly contacts must be used while also avoiding separation requirements between separate polysilicon lines. This sharing saves a significant percentage of the space of a single compact pixel layout. This flipping is shown in the upper right quadrant, Figure 42 (b). Additionally, alternating mirroring in the vertical direction can also be used to save even more space along a column. Vertical and horizontal mirroring are used together in the lower left quadrant, Figure 42 (c). In this scheme, transistors from separate pixels along a column can abut to share a single drain area. Unfortunately, grouping transistors between every other pixel creates a non uniform spacing of the photodiodes. This can have some adverse effects for small scale imaging algorithms.

To test the effects of alternating mirroring, the four layouts mentioned were created on a single fabricated chip. Although quadrants (a) and (d) have the same tiling schemes, quadrant (a) has the unique trait that the transistors were 1.8x1.8μm while the three other quadrants used 2.4x2.4μm transistors. Also, quadrant (c) also had a slightly larger photodiode area, taking advantage of the space saving using mirrored pixel layouts. Other changes in layout on this chip versus some previous pixel arrays were the use of more ground contacts in the pixel array and vertical transistors. Previous layouts had only one ground contact per four pixels and the transistors were horizontal. The difference is illustrated in Fig41. It was believed that having the transistors with the same vertical orientation with current flow in the same direction may improve matching statistics. Unfortunate results taken from the chip did not prove this to be true. Statistics did not show improvement, in particular voltage offset and photodiode current are shown in Table 2. Later, more detailed measurements with cleaner testing may reveal a small improvement but it is certain there are not large advantages or differences with these layouts. There are obvious effects, though, in some cases, if alternating routing creates uneven shielding.

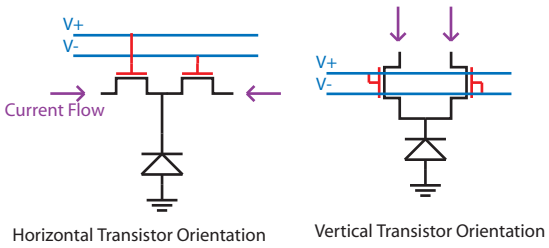


Figure 41. Vertical versus horizontal layout orientation for transistors of the differential pair

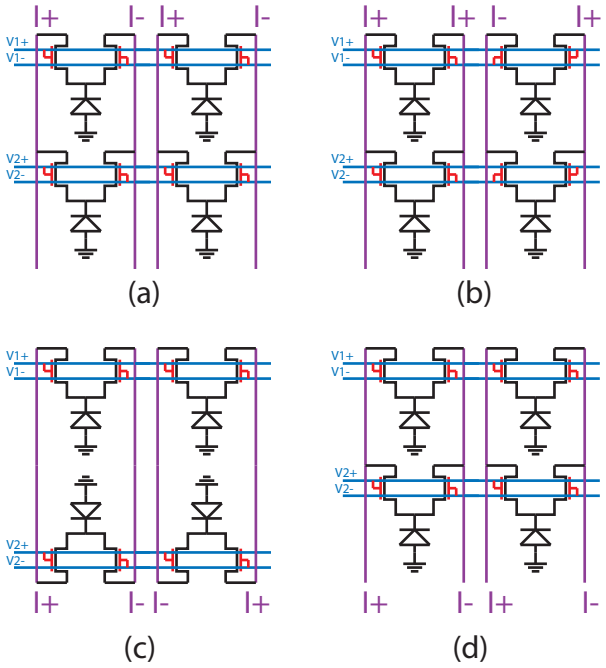


Figure 42. Schematic representation of layout to observe effect of alternating mirrored pixel layouts. Four 32x30 arrays on the same chip with different mirror schemes were used. The figure shows an orientation of a group of four from each quadrant. The upper left quadrant (a) used no alternating and had 1.8x1.8μm transistors. The upper right (b) quadrant had every other pixel along a row horizontally flipped and had 2.4x2.4μm transistors .The lower left quadrant (c) used flipping in the horizontal and vertical directions and had 2.4x2.4μm transistors and slightly larger photodiodes. The lower right quadrant (d) used no alternating and had 2.4x2.4μm trans.

Table 2. Layout Variation Statistics

Quadrant	Photodiode Current		V_{offset}		$\lvert V_{offset} \rvert$	
	Mean	Std Dev	Mean	Std. Dev.	Mean	Std. Dev.
(a)	201pA	5.713pA	-0.473mV	12.2mV	9.64mV	7.46mV
(b)	195pA	4.38pA	-0.106mV	10.4mV	8.49mV	5.95mV
(c)	229pA	3.97pA	-2.33mV	11.5mV	8.97mV	7.24mV
(d)	190A	2.62pA	0.113mV	11.1mV	8.98mV	6.57mV

CHAPTER 4

ERROR REMOVAL

The matrix transform imager currently suffers from several offsets which are expected in any analog system. Some source of the errors are mismatches in threshold voltages, photodiode sizes, parasitic diode junction leakages, and offsets in the readout circuitry. In APS imagers, double correlated sampling removes many of the offsets of the pixels and the readout circuitry. Correlated double sampling works by sampling each pixel twice during its integration phase [10]. Just as in Figure 4, the extraction of the pixel's light intensity becomes independent of the absolute offsets. There are also techniques that use double sampling, which still involves two samples, but not necessarily during the same integration cycle. To remove offsets, double sampling schemes can be applied to this transform imager's design. The techniques involves taking the difference of two results. This design can also be related to frame differencing such as in [11].

Most pixel error can be modeled as a gain and offsets error. For simple imagers, a post correction can be performed to remove the gain and offset errors in the resulting image if the pixels can be characterized. In this transform imager architecture the problem is not as easily solved. The output of the imager is not a image but rather a result of a computation on the image. Removing errors is not as easy then. For instance, if the imager sensors have offsets such as dark currents, those offsets are transformed along with the imager. Since the transforms here are linear one can compute the transform of the offsets and remove it from the results. This removal must occur before any non-linear post computation, such as thresholding in JPEG compression, if they are to be removed completely. Noise can significantly effect the performance of compression algorithms. Gains errors are even more difficult to remove. They effect the transform itself and can cause errors in the result that are non-invertable. Moving error correction to the pixel itself such as in [12, 13] where floating gates are used would work since it removes errors before the transformation occurs. This

comes at the cost of resolution or fill factor.

4.1 Double Sampling

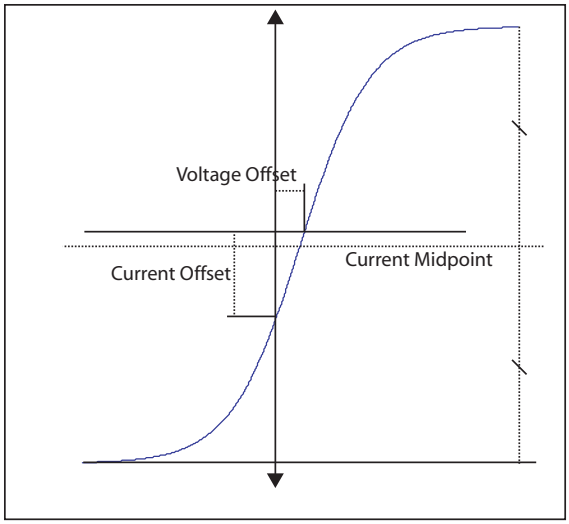
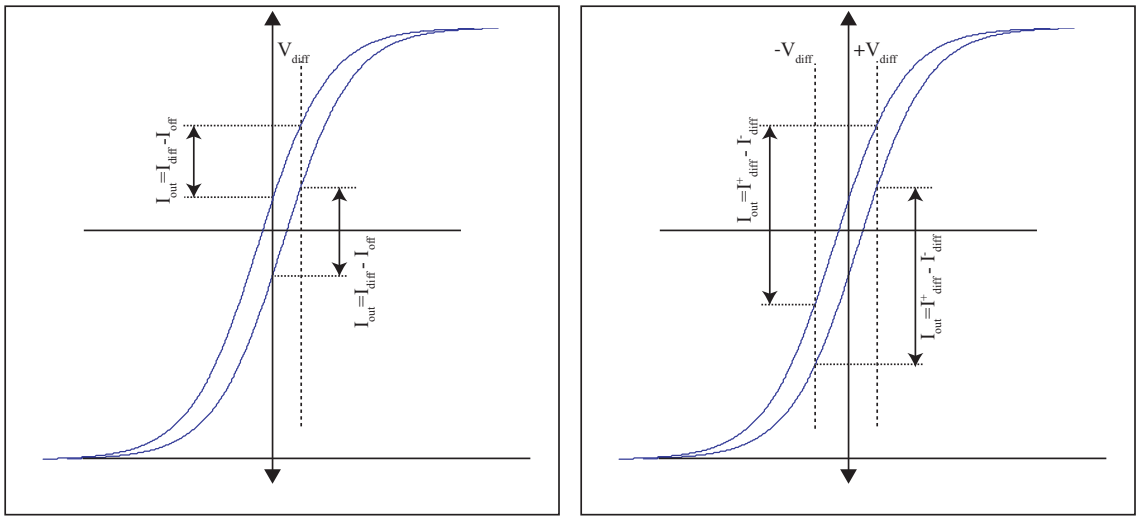


Figure 43. Voltage and current offsets in individual pixels.

As seen in Fig. 43, each pixel has an offset voltage and current. Along a column these offsets culminate into a large column offset. Therefore each pixel has its own unique offset in addition to the offsets of the column and readout circuitry. A double sampling scheme in this imager must be suited for canceling offsets of groups of pixels used together. A combination of offset removal techniques is also sometimes useful.

When reading a value from the differential pixel, the absolute value of the differential current is not the value representative of the pixel output since several large offsets affect this value. The idea presented here is to take a difference of two readings to account for the offset. Figure 44 (a) shows curves from two pixels with different voltage and current offsets but with the same illumination. When V_{diff} is applied to the differential inputs of the pixels each pixel would return a different differential output. However, if at each pixel the output at $V_{diff} = 0$ was also taken and then subtracted from each respective output, the offset corrected results would be the same. Alternatively, one could take one measurement using V_{diff} and a second using $-V_{diff}$ as Figure 44 (b) illustrates. Creating $-V_{diff}$ simply



(a) (b)

Figure 44. Double sampling can be taken from the subtraction of two reads. The two curves simulate two pixels under the same illumination but they have different offsets. (a) illustrates current differences taken applying differential voltages of zero differential and V_{diff} differential.(b) illustrates current differences taken applying differential voltages of V_{diff} differential and $-V_{diff}$ differential. Double sampling rejects the offsets.

involves switching the differential inputs.

Now, this imager architecture is best used as a transform imager, meaning that it is design for groups of pixels to be read at once. In this architecture there are a few options for reading a raw image. First, the notion of an off pixels and on pixels should be introduced. On pixels are those in the currently selected blocks. They receive the bias coefficients which have a common mode V_{com}. The coefficients are conveyed in the difference of the voltages. The off pixels are those in the unselected blocks. Typically the all of the off pixels have there differential inputs all tied to one common voltage referred to as V_{off}. V_{off} may be set as V_{com} for speed reasons or set to ground to reduce the contribution of all the pixels in a column that are not being read from. When trying to obtain a direct readout of the image and not a modified image, an identity transform would be used. An identity transform is a special case where only pixel in a row is read at a time. So the zeros in the identity matrix could be set as either V_{com} or V_{off}. The general case for the transforms is that all the coefficients including zero are generated using a common mode V_{com}. For double sampling

two matrices would be applied and the results would be subtracted. The example of using an identity matrix to read the image will be given here. For the technique illustrated in Figure 44 (a), first a zero matrix, Equation 13, would be used to read the offsets, and then an appropriately scaled identity matrix, Equation 14, would be used to read the image. The results from the zero matrix read would then be subtracted from the image read. M_{zero} has the nice property that all of its column vectors are the same so only one read must actually be performed for this matrix. The technique illustrated in Figure 44 (b) involves reading one image using an identity matrix , Equation 14, and then a differentially negative version of the identity matrix, Equation 15. These are then subtracted to get the final result.

$$M_{zero} = \begin{bmatrix} V_{com} & V_{com} & V_{com} & V_{com} \\ V_{com} & V_{com} & V_{com} & V_{com} \\ V_{com} & V_{com} & V_{com} & V_{com} \\ V_{com} & V_{com} & V_{com} & V_{com} \end{bmatrix} \tag{13}$$

$$M_{plus} = \begin{bmatrix} V_{com} + \frac{V_{diff}}{2} & V_{com} & V_{com} & V_{com} \\ V_{off} & V_{com} + \frac{V_{diff}}{2} & V_{com} & V_{com} \\ V_{com} & V_{com} & V_{com} + \frac{V_{diff}}{2} & V_{com} \\ V_{com} & V_{com} & V_{com} & V_{off} + \frac{V_{diff}}{2} \end{bmatrix} \tag{14}$$

$$M_{minus} = \begin{bmatrix} V_{com} - \frac{V_{diff}}{2} & V_{com} & V_{com} & V_{com} \\ V_{com} & V_{com} - \frac{V_{diff}}{2} & V_{com} & V_{com} \\ V_{com} & V_{com} & V_{com} - \frac{V_{diff}}{2} & V_{com} \\ V_{com} & V_{com} & V_{com} & V_{com} - \frac{V_{diff}}{2} \end{bmatrix} \tag{15}$$

To aid in subtraction, the negation one of the results can be obtained by switching the differential outputs of the imager. Figure 45 shows the architecture of a fabricated chip used to implement these offsets removals. For this chip, the final difference of the differential channels is actually computed off-chip using a subtraction amplifier circuit.

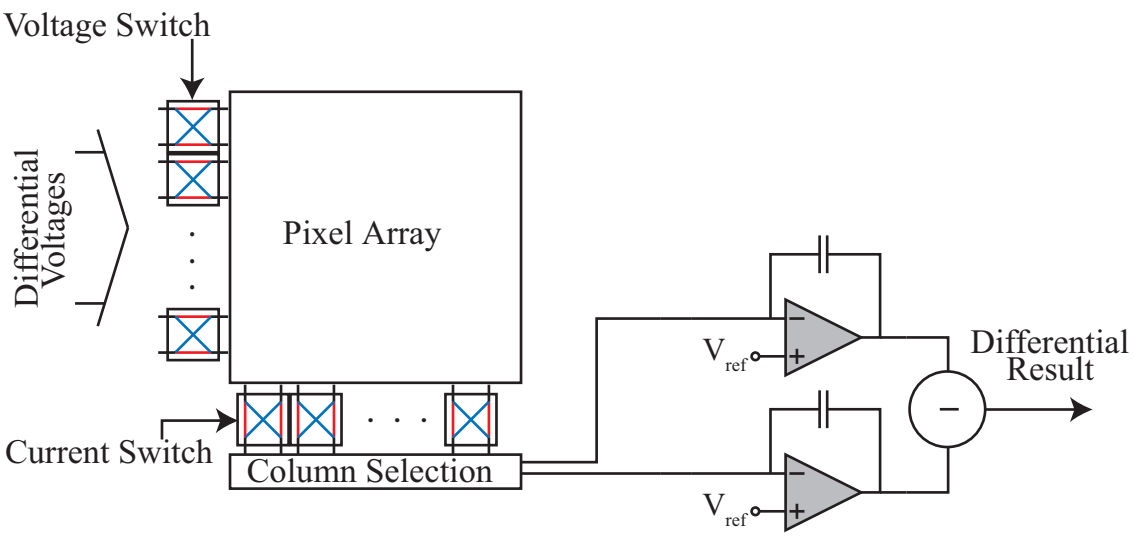
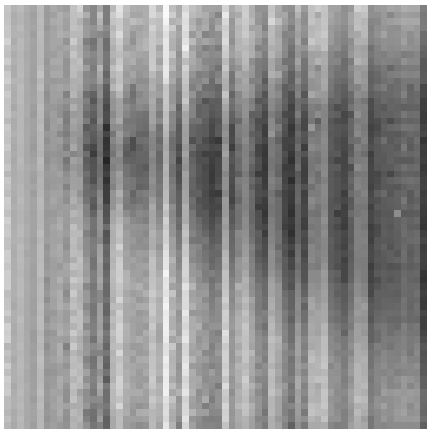


Figure 45. Switch imager design for double sampling and and dual slope integration.

Figure 46 shows some of the first results from reading an image. A picture of a cardboard in a roughly triangular shape was imaged in the foreground against the bright ceiling in the background. It may be important to note that the image was not in good focus, so the blurry image is not a result of the imager. The triangular shape was used to illustrate an important point in removing column offsets. Figure 46(a) shows a standard image read using a full rail difference on differential pair,approximately 3.3V and 0V, with $V_{off} = 0V$.Figure 46(b) shows the same image read with the differential voltages and currents switched in polarity. The voltages are flipped on chip using switches placed just before the pixel array. The currents are flipped just after the pixel array. Switching the currents produces a negative result so that adding the two results becomes an addition. The expected column offsets are clearly visible in both of the images. Comparing Figure 46(a) and Figure 46(b) reveals that flipping both voltage and current negates the column offsets while maintaining the polarity of the image. The image is effectively negated twice while column offsets are negated once. Figure 46(d) shows a result much more representative of what the image should be. It is created by adding the results of Figure 46(a) and Figure 46(b), which have opposite offsets but the same underlying image.These results confirm the expected behavior of the



Standard image read
(a)

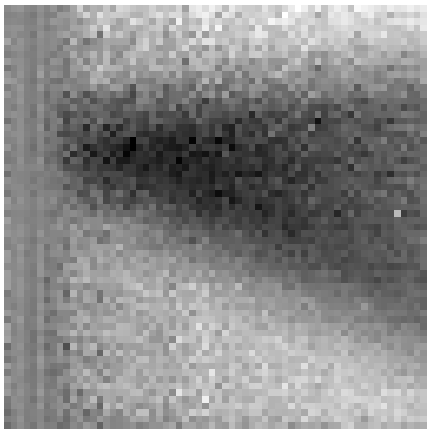


Image from (a) with column average removed
(c)

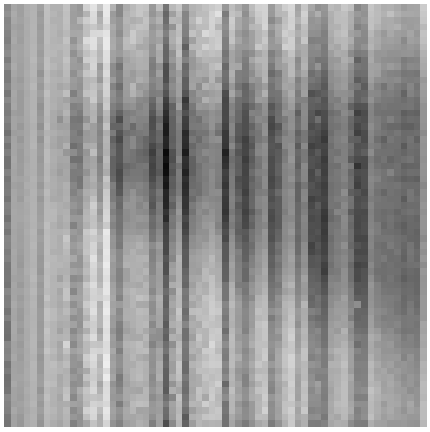
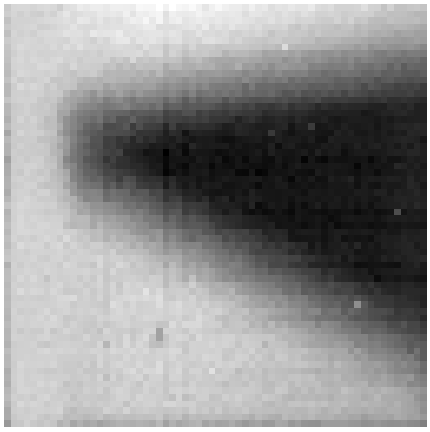


Image read with fliped voltage and current
(b)



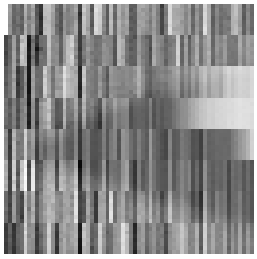
Addition of (a) and (b)
(d)

Figure 46. Results reading of a raw image. (a) is a standard positive read showing column offsets. This is done outside the linear range of the diff pair (b) shows the same image with input voltages flipped and output currents flipped. The image maintains its polarity while the offsets are negated. (c) Is an attempt to remove offsets using column DC removal but it also removes the column DC of the desired image. False darkening on the left and brightening on the right occurs. (d) Shows the addition of a and b to remove offsets without removing the desired DC of the actual image

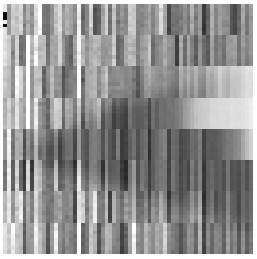
imager array and its offsets.

46(c) shows the results of an attempt to remove the offsets of the image in Figure 46(a) by removing the average of each column. This attempt initially may seem reasonable since the column offsets is almost a constant along a column and acts as a DC offset. However, doing this also removes the DC of the image itself which is undesirable. The triangular shape helps to emphasize this effect since the resulting image should not have the same average or DC for each column. The leftmost columns should have the lightest column averages but they were darkened by the the DC offset removal technique. The rightmost columns should have the darkest averages and instead are artificially lightened. As Figure46(d) shows, the double sampling technique does not suffer from this problem.

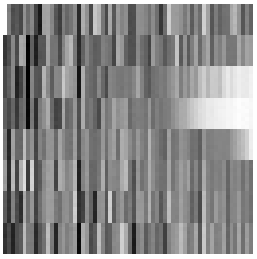
Figure 47 shows results of working in the linear region. Figure 47(a) is the normal read using an identity matrix scaled to be in the linear region of operation. Figure 47(b) shows a read with differential input voltages switched and differential output currents switched. Again, in (b) the image maintains its polarity and the offsets are negated. But, there is an additional anomaly on the right side of the images that shows up as a bright area in the image. A read using a zero matrix (c) shows the same anomaly. Adding the results of the positive and negative read cancel most of the offsets but the anomaly remained, Figure 47(d). Using the zero matrix to remove offsets produced very good results, 47(e). The results in (d) are better except in the region of the anomaly. The anomaly and the artificial edges near it are like due to a non linearity problem with the I-V converters on the chip when currents are low. Since the right hand side of the image has the lowest currents it became a problem though. Figure 48 shows results of a DCT transform and using the zero matrix to remove the offsets. Once the linearity problem is corrected, using positive and positive reads may produce even better results.



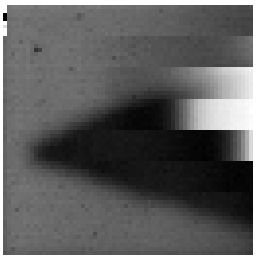
Positive Read
(a)



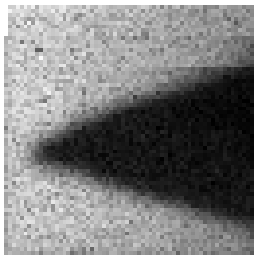
Negative Read
(b)



Zero Read
(c)

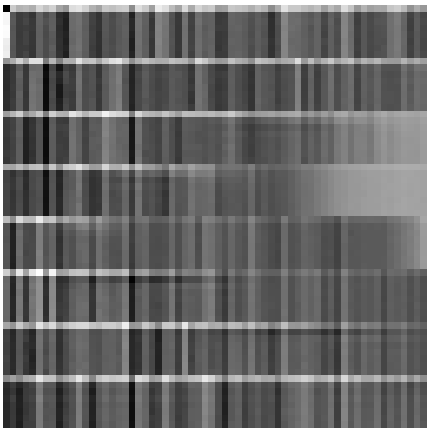


Switching Compensation (a)+(b)
(d)

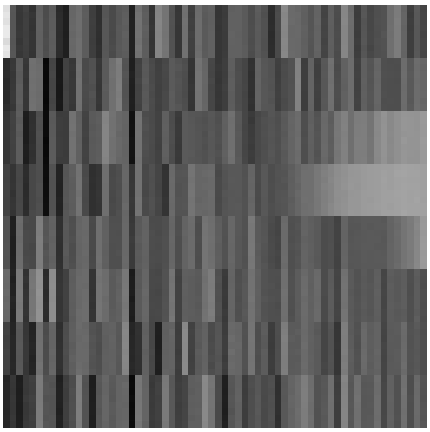


Zero Compensation (a)−(c)
(e)

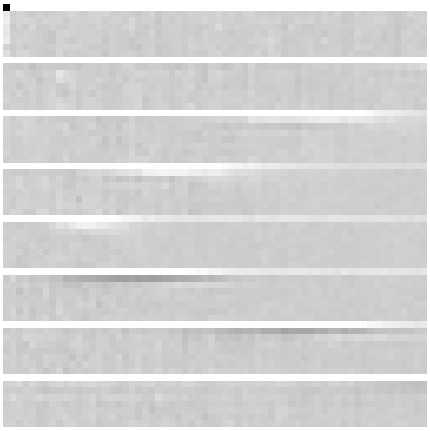
Figure 47. Result reading a image using an identity matrix transform in the linear region with off blocks set to 0V common mode. (a) shows an image read using the identity matrix and (b) shows the results using a negative identity matrix and negated outputs. (c) shows a read using a matrix of all zeros (1.5V common mode). (d) shows the result of the addition of (a) and (b). The white anomaly on the right hand side is likely a result of the I-V converter's nonlinear response which can be fixed in a future design. (e) shows zero matrix correction using (a)-(c). This avoided the white artifact but , as in (d), some false edges occur at the block boundaries, also likely due to the nonlinearity of the I-V converters.



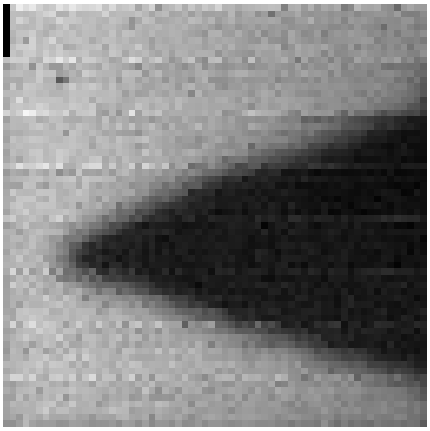
Raw DCT 1−D
(a)



Zero Matrix Read
(b)



DCT − Zero Matrix
(c)



Recontructed Image from (c)
(d)

Figure 48. DCT offset removal results using a zero matrix read. (a) shows as 1-D DCT computation and (b) shows offsets read using a zero matrix. (c) shows the transform with the offsets removed and (d) shows the result of performing an inverse DCT on (c).

4.2 Dual Slope Integration

The ability of the chip in Figure 45 to reverse the polarity of the output was originally conceived to allow a more complete on chip implementation to remove offsets. Since reversing the polarity of the outputs negates the output and a temporal integration implements a summation, this chip can implement the subtraction of two results on chip. The outputs of the two integrators are show in Figure 49 along with an amplified and offset subtraction of difference of the two. To begin, the appropriate row of the input voltage matrix is applied to the imager. The reset of the integrators is released to begin integration and this continues for some time. Then, while still integrating, the input voltages and output currents are reversed in polarity. After an equal integration time the outputs are sampled. So, the results of the positive and negative versions of the input are created on chip and the results are subtracted temporally.

Though it is difficult to see, the slopes of the differential outputs changes slightly before and after the polarity is flipped. This is because the desired signal is riding on a large common mode current. The large offsets current complicated offset removal. The feedthrough effects of the switches can be seen at the polarity switching time. Since these effects are proportional to the large offset component of the output, the errors can be large compared to the desired signal. The hope is that they can at least be made constant so that removing the effects becomes more achievable. There are also some non-linear effects in the amplifier used in the integrator. The initial curvature does not actually effect the final result as long as the integrators reach a linear region before they are read.

Figure 50 shows a comparison of results taken from the imager. Figure 50(a) shows results using the dual integration method discussed here while Figure 50(b) shows results taken using two separate integration cycles. Though the dual integration removes most of the current offsets, it seems that double sampling with two separate integration cycles produced better results. This should be expected since nearly all offsets are produced identically in the two integration cycles and thus would be canceled out better then doing one

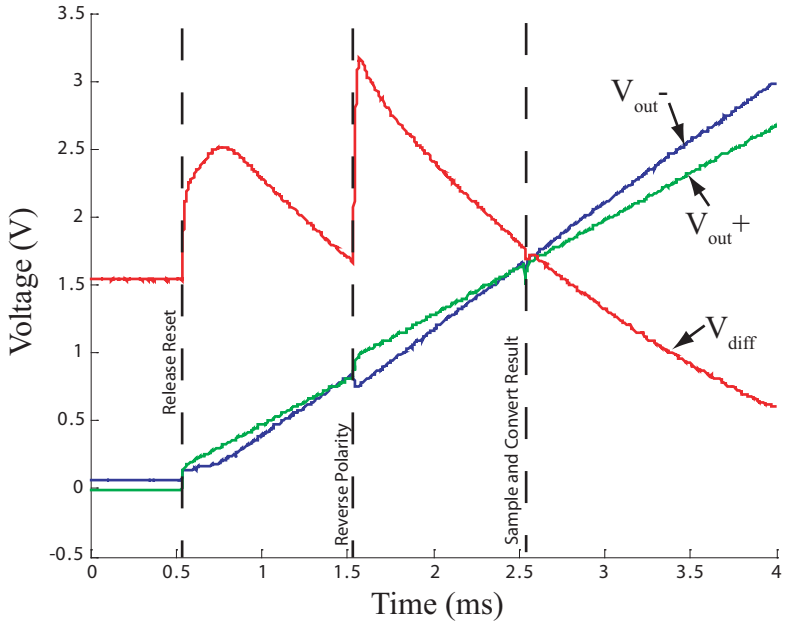
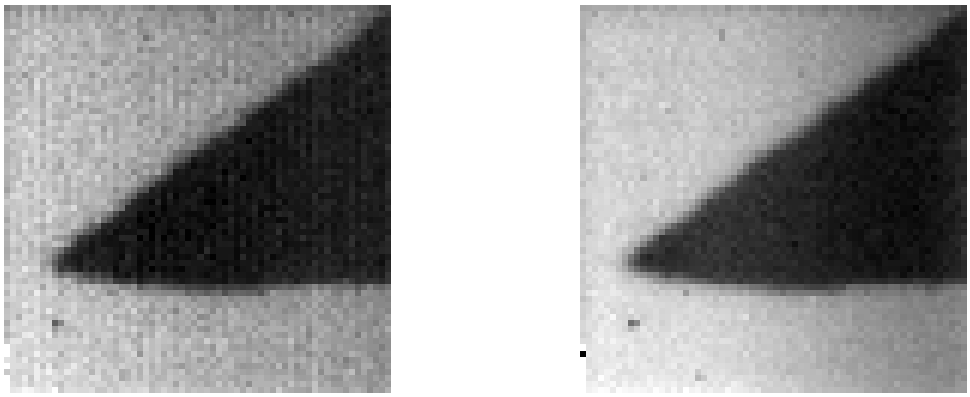


Figure 49. Dual slope integration voltage outputs.

integration cycle. Further circuit design including improving the linearity of the output amplifiers and reducing feed through effects may narrow this margin.



(a) Dual−Slope Integration (a) Double Sampling

Figure 50. Dual Slope Integration vs. Double Sampling results.

CHAPTER 5

LIGHT ADAPTATION

As previously mentioned, imagers can encounter a wide range of light intensities, even within the same image frame. The human visual system has several mechanisms to adapt to environmental light levels which everyone experiences walking outdoors or indoors on a sunny day. To mimic this ability in imager sensors, approaches have been explored. Some placed adaptation circuitry directly in the pixel itself [14], which adapts its output DC level slowly to account for changes in average light intensity while responding acutely to fast changes. This adaptation allows the sensor to adjusts its usable input range, providing a mechanism for dynamic ranging. The circuit also takes advantage of a logarithmic compression mechanism in Figure 1(b). Other methods uses multiple integration cycles at varying gains and/or varying exposure times [6, 15, 16] to deal with these issues.

To study how to account for these offsets a light adaptive readout circuit was designed and fabricated. Figure51 shows the basic imager blocks and how the designed light adaptive circuitry fits into the architecture as a readout amplifier. Figure 52 presents the blocks that make up the adaptive readout circuitry. The differential inputs from a row of the pixel array are connect the a current input amplifier which implements a cascoded input to minimize voltage swing on the row line. This circuit is shown in Figure53. The amplifiers uses a gain control V_{adapt}. The output voltage is fed to a min-max detection which is shown in Figure54. The min and max detection are performed using diode connected transistors and a capacitor. Also included are leak transistors which control how long detected values are held. This stage does suffer from diode drops and a voltage division occurring with the series resistance of the diode transistors and leak transistors. The min and max voltages are then connected to a GmC filter with floating gate inputs. The GmC filter is shown in Figure55. The GmC stage utilizes floating gate transistor inputs to allow tunning of the output DC level which sets the overall gain of the system. The programmable inputs

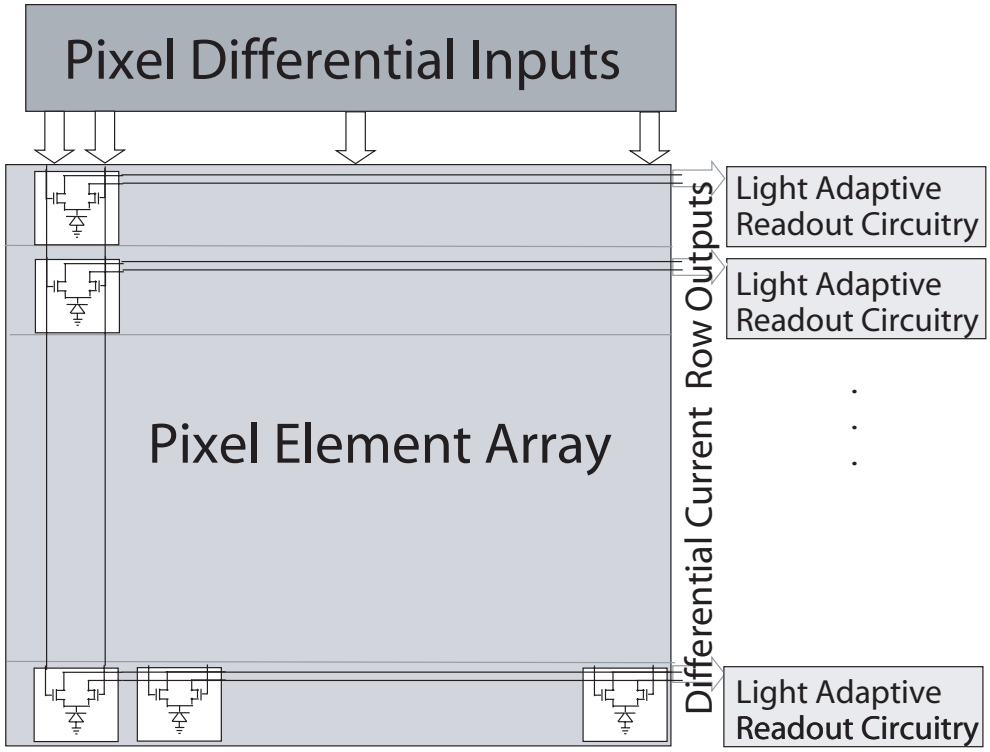


Figure 51. Light adaption imager architecture

also allow for compensation of the diode drops in the min max detectors. The GmC filter implements a low-pass response for the adaptation.

This chip still remains in the testing phase. The min-max circuits were tested successfully but other portions of the chip were not, though they did work in simulation. Even so, this study did reveal the complexities and possible advantages of producing a readout circuit which could adapt to DC and AC magnitudes. The mean and variance of an image are not always correlated over time. Adapting the analog readout circuitry to respond to these parameters independently can allow for better imager sensitivity. The exact placement and implementation of the light adaptation will need to be studied further.

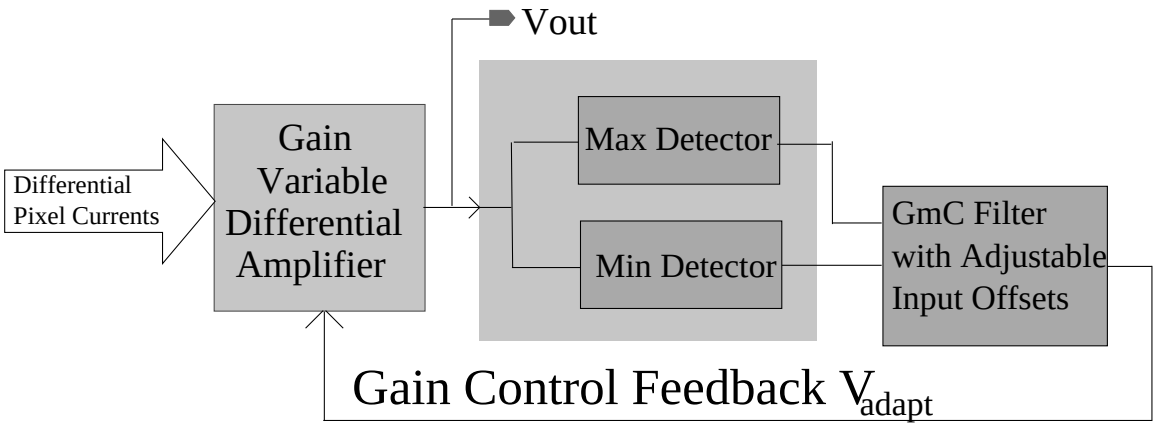


Figure 52. Light adaptation output block diagram

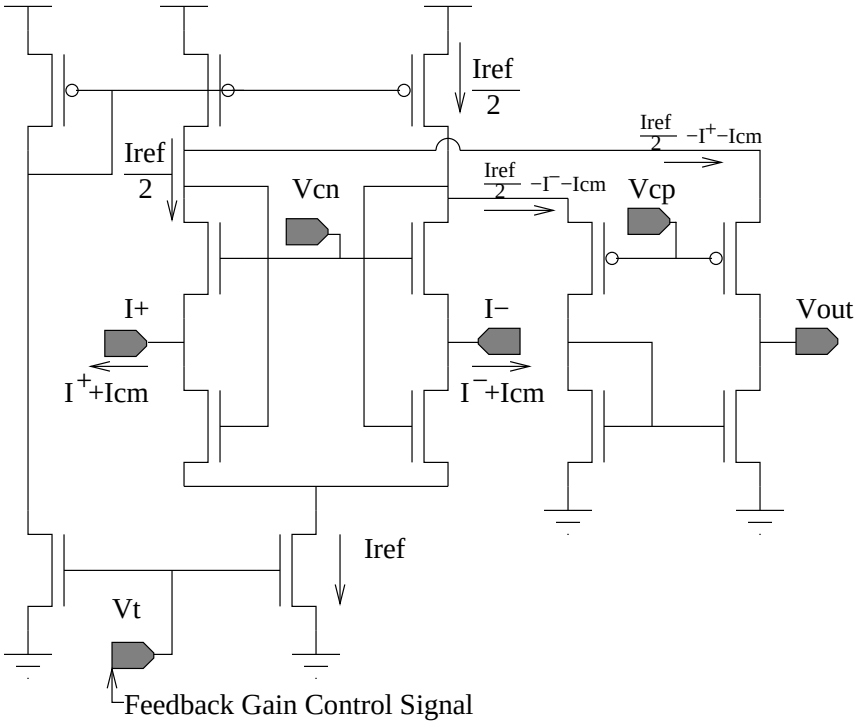


Figure 53. Light adaptation folded cascode current input amplifier with gain control

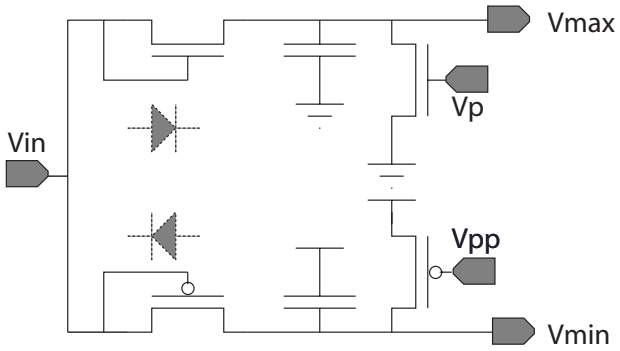


Figure 54. Min-Max detectors implemented using diode connected transistors.

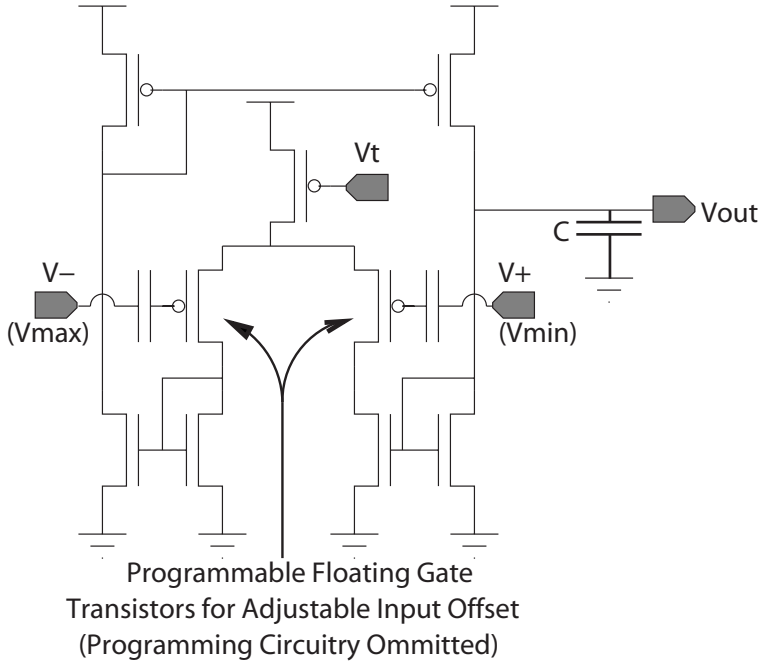


Figure 55. Floating gate input OTA used in a GmC filter.

CHAPTER 6

MEGAPIXEL IMAGER

The transform imager is clearly a scalable architecture in many respects. The pixel count can be increased and number of stored transforms can be increased. Several other variations on the design can occur as well. Logically, smaller implementations of this architecture were first designed and tested. But, when dealing with physical chip design, scaling up the implementation is not usually straightforward and often involves a redesign of certain components. With gained knowledge of the operation of the pixels and experience from previous imager designs, a larger imager was designed and fabricated. This chapter overviews the design which awaits testing.

6.1 Top Level

Figure 56 shows the blocks of the megapixel imager architecture. Taking into account the studies of previous imagers, this imager was designed for larger pixel counts. It is important to note here that this pixel array is rotated 90 degrees from previous layouts. Voltages inputs are shared down columns and output currents are tied along rows. The input bias generation uses floating gate technology to store analog coefficients for several block transforms. This block feeds voltages to the array with active amplification. The block selection circuitry then selects one column of blocks to apply the coefficients to while the rest are turned off. Now, the input selection circuitry also has the ability to switch positive and negative voltages, which may be useful for several reasons including characterization, signal modulation, or offset removal. The pixels were redesigned to fit in a smaller size of 4.35 $\mu m^2$with reduced row parasitic current and capacitance. The output current go to switches which can switching positive and negative currents to the next stage, much like the voltage switching on the input. Row amplifiers are then used as active cascodes for the pixel array while providing a buffered voltage output. One block of the output amplifiers is

selected at a time for output to the offset removal stage which allows offset compensation individually for each block of outputs. This utility is implemented by switching between floating gates based on which row is selected. The vector of outputs of the compensation stage are then fed to a vector matrix multiplier which then feeds to A/D converters. The converters in this version are 16 single ended converters. Obviously future designs will benefit from design and use of 8 differential converters.

6.2 Input Sections

Figure57 shows one of sixteen programmable amplifiers in the input bias generation stage. It is fundamentally a nine transistor PFET input amplifier where one of the input PFETs is replaced by several floating gate PFETs which are selected one at a time. Each floating gate PFET is programmed with an individual offset which sets the appropriate output voltage. The difference between V_{bias-} and V_{bias+} will set the DC voltage on the output while the charge on each floating gate will control variation of the output. Since the block sizes on this chip are 8x8, there are eight differential voltage pairs needed at a time, hence the need for 16 of these programmable coefficient generators. This method essentially requires two floating gate PFETs per coefficient. This is not necessary though. One could imaging using eight programmed voltages and then use circuitry to generate corresponding differential voltages with a desired common mode. Each method has advantages. In this design each coefficient generator has 32 floating gate transistors. This allows for storage of four 8x8 matrices. The proper group of 8 floating gate transistors are cycled through to produce the desired transform.

6.3 Pixel Array

The pixel was redesigned to accommodate the larger array size. Since a photodiode conducts current under light even with no voltage across it, it is very difficult to turn it completely off in the differential pixel design. Even if the voltages on a differential pair are tied

to ground, the photodiode will generate a negative voltage on the source of the transistors allowing them to turn on. Since each row has 1024 pixels, a very large row current would be generated. Measuring the outputs of 8 pixels is difficult when 1016 other pixels are generating current on the the line. To divert the current of the pixels which are turned off, 4 extra transistors were added per 8 pixels as shown in Figure 58. The current from each group of 8 pixels is either connected to the row output line through the set of second level transistors, or the current of the block is diverted to an off line. This scheme also limits the total capacitance on the output line since each off block only contributes a single drain capacitance instead of 8. To also help with the effects of the large row capacitance, the output amplifiers implement an active cascode to maintain a constant voltage on the large line. Minimizing the voltage changes on the line prevents large charging and discharging of the line capacitance which is especially slow with small photodiode currents.

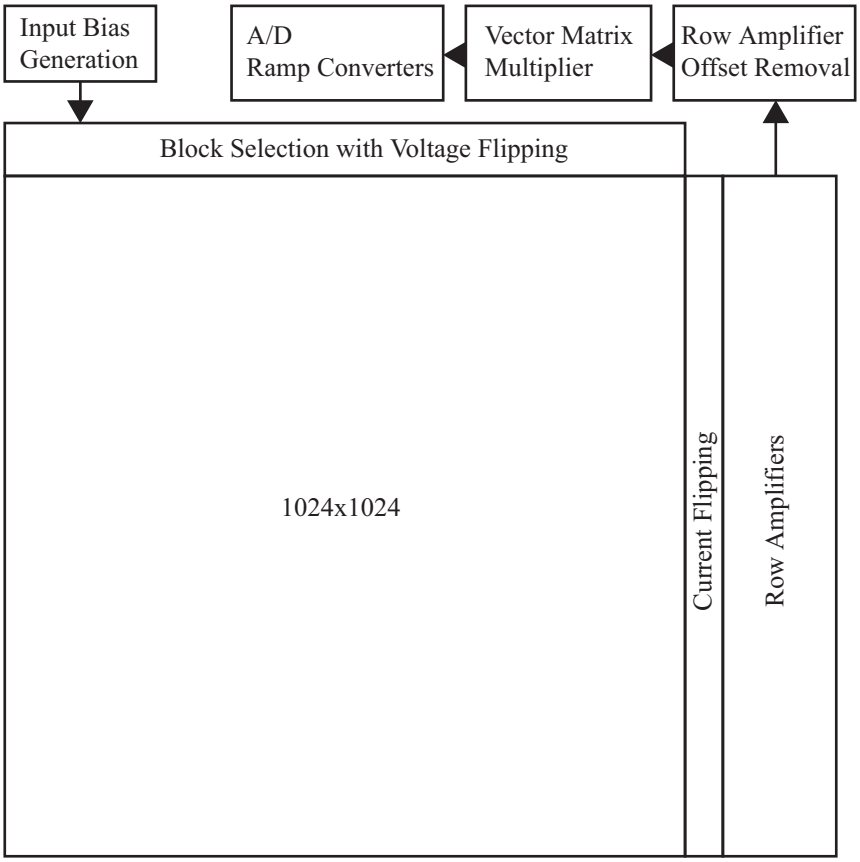


Figure 56. One-megapixel imager top-level blocks

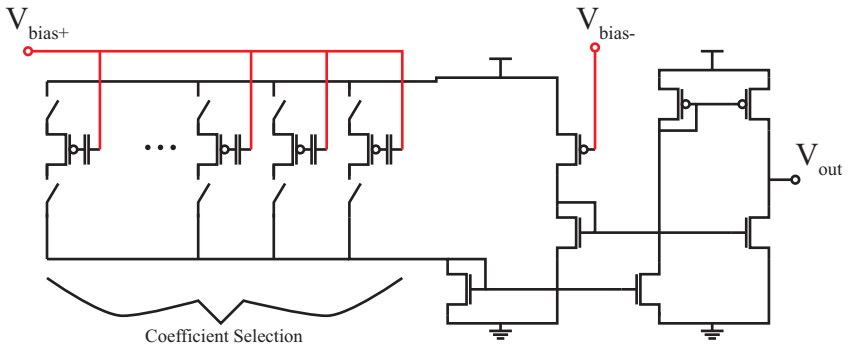


Figure 57. Input coefficient generation using analog non-volatile floating gate transistors.

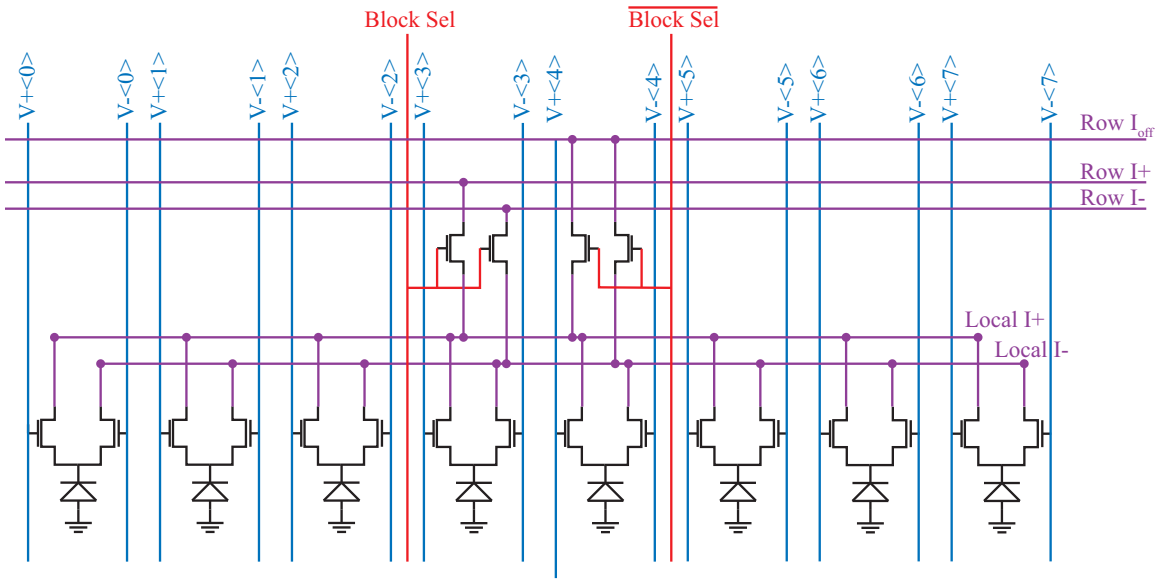


Figure 58. Pixel group design to reduce row offsets and row capacitance.

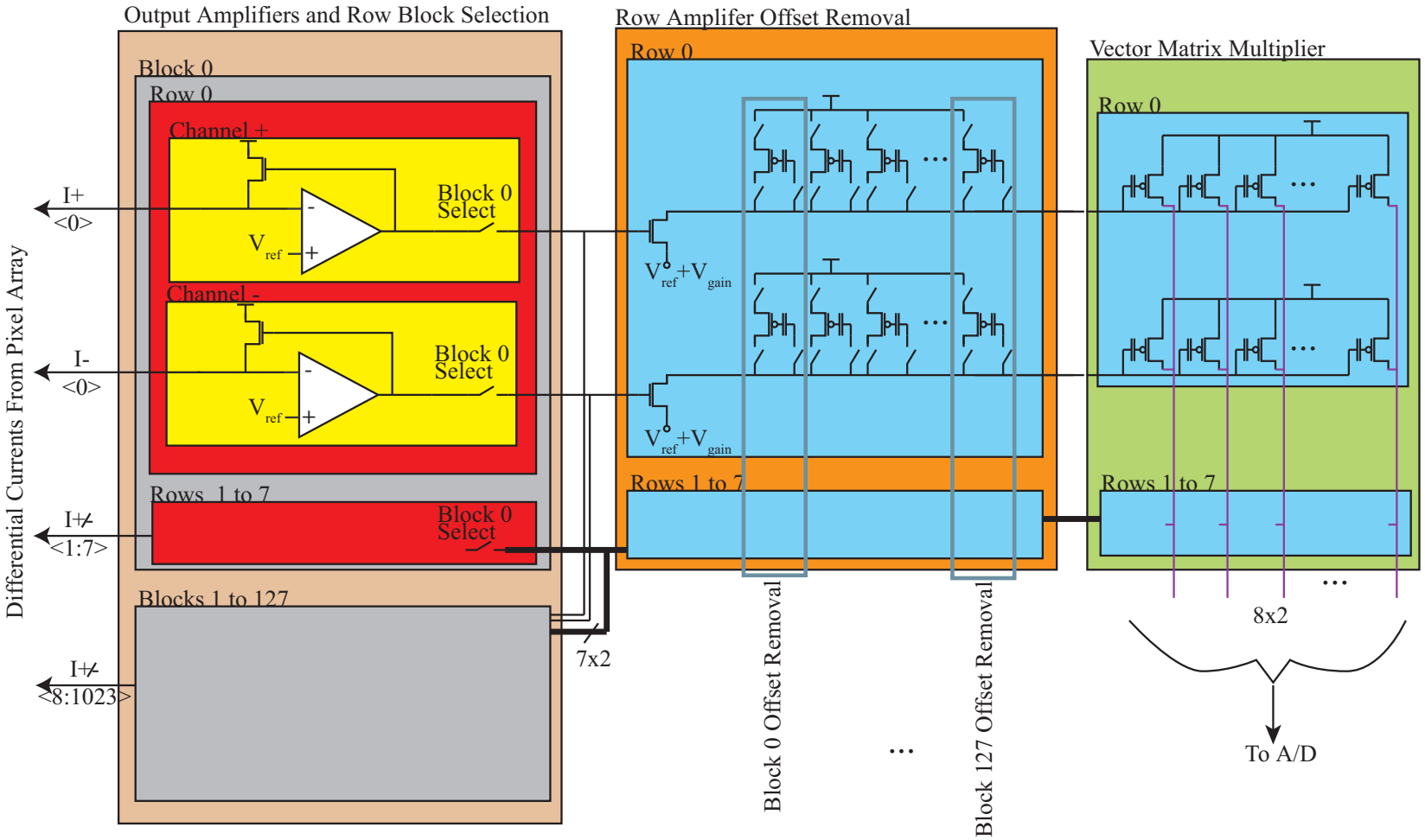


Figure 59. Output blocks for megapixel imager.

6.4 Output Sections

The output portion of the imager is shown in Figure 59. The output amplifiers set the voltage on the row output line to V_{ref}, with some undesired offset voltage, which is also the source voltage of the feedback NFET. The output of the amplifier is the voltage on the gate of the feedback NFET which is fed to the offset removal stage. Here an NFET receives the same gate voltage so that it mirrors the current on the row of the imager. The source of this NFET is set to $V_{ref} + V_{gain}$. V_{gain} can be used as a global gain control for the mirrored currents. This allows for a gain control to move depending on global image light levels. While in this design the gain control is manual, this may be used to facilitate an automatic gain control. In this offset removal stage, a column of diode connected floating gate PFETs is selected corresponding to the block of outputs selected. This allows individual offsets compensation for each amplifier of each block. It also allows compensation of the offsets between the feedback NFET and the NFET in this offset stage. These diode connected floating gate transistors produce a voltage output. The vector matrix multiplier then receives these voltages. Each row of the vector matrix multiplier has several corresponding floating gate PFETs which in parallel mirror the currents in the offset removal stage, but each with a programmable gain. So the vector of inputs from the offset removal stage is multiplied by the matrix of programmed coefficients. Each differential multiplication requires four transistors for the four quadrant multiplication. Therefore, there are 16 rows in the multiplier each with 16 transistors. To store more then one transform, each row would have to have 16 transistors for each transform. The corresponding transistors or outputs could be selected based on the desired transform.

The chip also includes 16 single-ended integrating A/D converters. The currents are integrated on capacitors. Counters and comparators time how long it takes the voltages to reach a threshold. For better resolution and speed on future design iterations, differential converters will be needed. These converters provide a digital output, completing an all digital interface to the chip, excluding the several analog bias voltages needed for this

prototype. These voltage biases could also be stored internally using floating gate storage.

CHAPTER 7

CONCLUSION

This paper has presented a body of work in progress to understanding and developing better CMOS imagers. In particular, the operation of the pixel element of the CMOS transform has been studied. The operation has been verified and characterized on processes including 0.5, 0.35, and 0.18 micron processes. When trying to improve the quality of these imagers, the studies here provide confidence in the operation of the pixels and knowledge of errors and mismatches. Some errors, such as column or block offsets have been identified as image dependent transient errors which will require some creative multiple sampling of the image. Some error removal attempts have been described here which will no doubt lead to other improved techniques. The double sampling obviously worked well in removing the largest component of the offsets in the results. Also studied were light adaptation and the need for the ability to dynamically adjust the response of the system. The newest imager has an analog global gain adjustment to work toward this end. Intelligent, automatic gain control should follow. The newest megapixel imager presented also incorporated other enhancements as a result of these studies.

With a better understanding of the nature of the errors and their statistical distributions it should become possible to estimate the performance of certain algorithms and techniques based on this imager. Also, the success of future removal techniques may hing on some of these statistical distributions. For instance, though a few pixels have voltage offsets that are very large, it is not likely that more then one pixel in a given block will be among these outliers. In this case, performing two reads per block with two different voltage offsets may reveal a single pixel error and account for it. Accounting for “dead” pixels is a issue in most imagers though. Knowing the distribution of errors will be key in any signal processing done with this imager. With an understanding of error components in the imager and gained experience in measuring them, a better characterization chip will likely

be developed, designed specifically with on-chip measurements to refine the accuracy of these statistics.

Future work will likely involve more iterations of the imager design. Error compensation circuitry will be added wherever possible and helpful. It may also become essential to develope algorithms which take into account the performance of the system. As stated before, the architecture is very flexible and need not be limited to block transforms. General convolutions, correlations, multi-resolution processing, and various feature extraction abilities may be added and will likely be the target of future work.

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